



The University of Aizu

Designing Neuromorphic Computing on FPGA

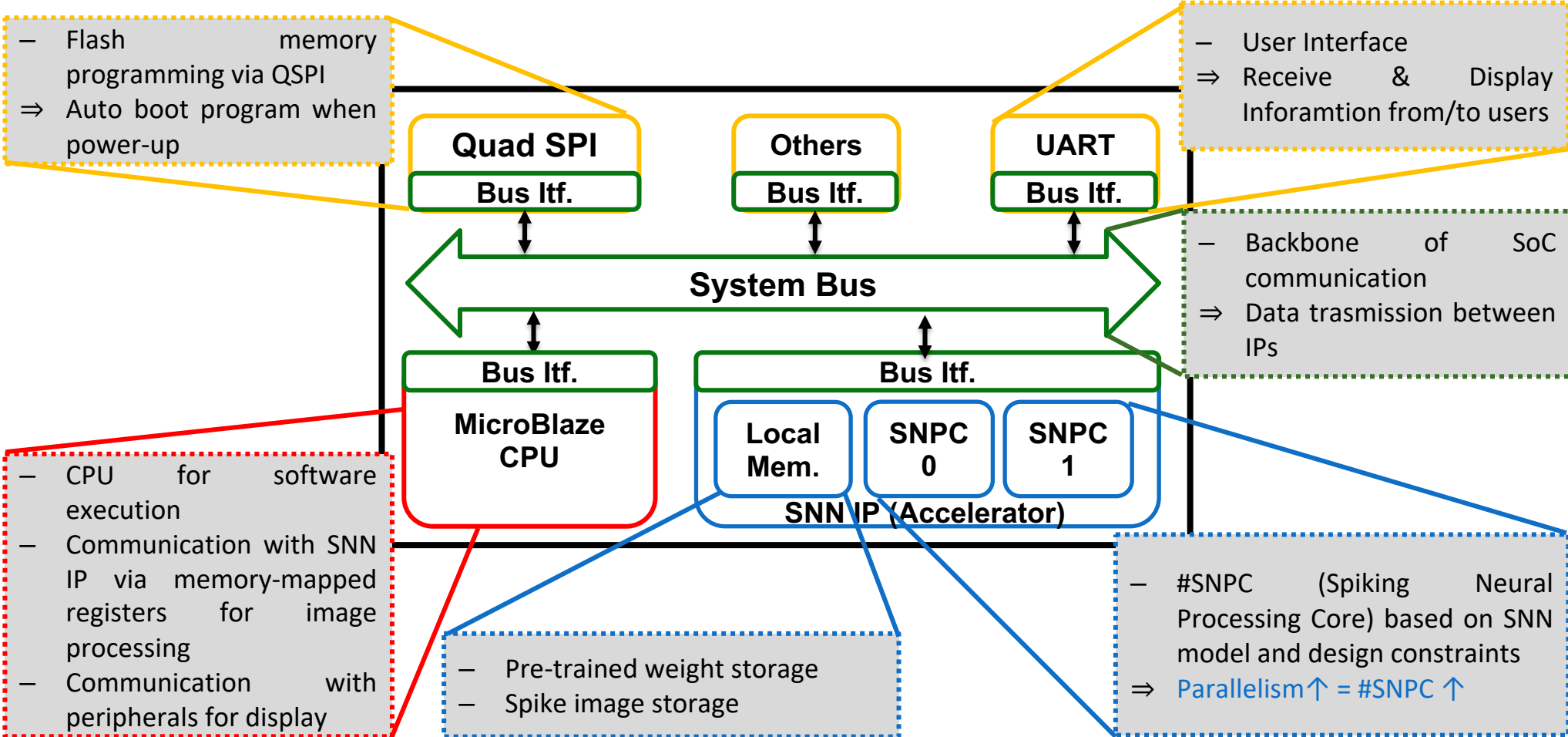
Contact person: DANG Nam Khanh

Office: 204-I

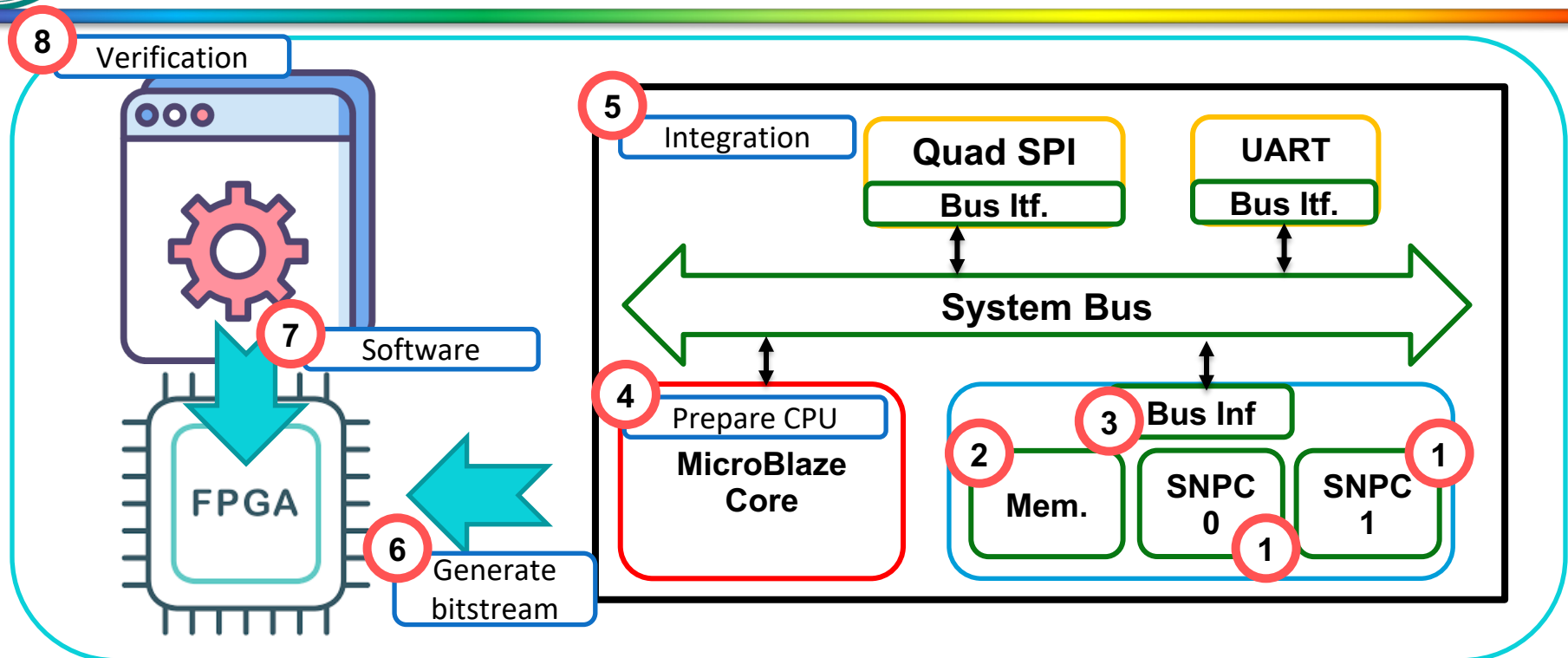
Email: khanh@u-aizu.ac.jp

Overview DN-SoC Architecture

- **Goal:** Domain specific + Hardware/Software co-design



FPGA Implementation Flow



1. Customize SNN IP based on design constraints
2. Implement local memories for trained weights and spike images
3. Implement bus interface for SNN IP & package this IP
4. Implement CPU core for software execution

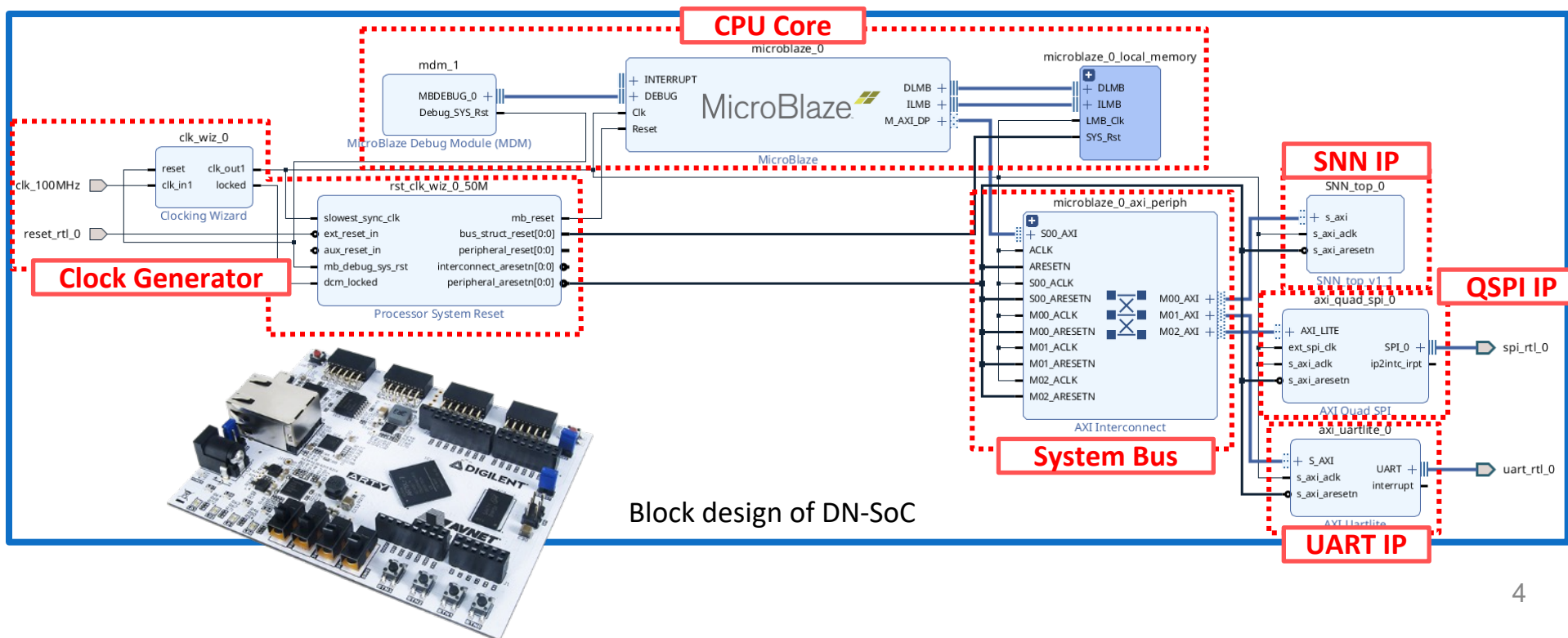
5. Integrate SoC together with CPU, SNN IP, system bus and peripherals
6. Generate bitstream of corresponding SoC
7. Develop software program with the associated hardware
8. Verify the developed SoC along with its software programs

DN-SoC Block Design

- DN-SoC Development using Xilinx Vivado tools with Arty A7 100T Dev-kit

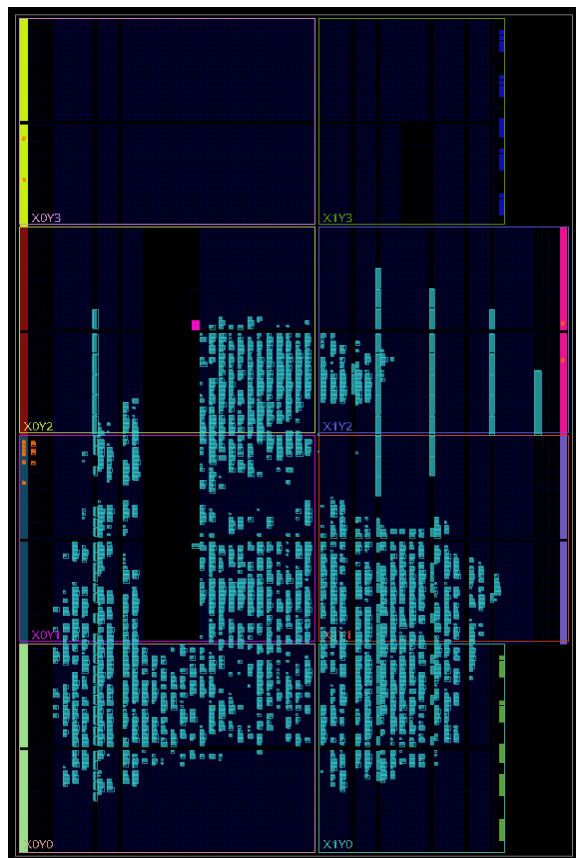
- Frequency: 50MHz
- Baud Rate: 115200
- System RAM: 128kB (0x00000000 - 0x0001FFFF)

- SNN Address: 64kB (0x44A00000 - 0x44A0FFFF)
- UART Address: 64kB (0x40600000 - 0x4060FFFF)
- QSPI Address: 64kB (0x44A10000 - 0x44A1FFFF)

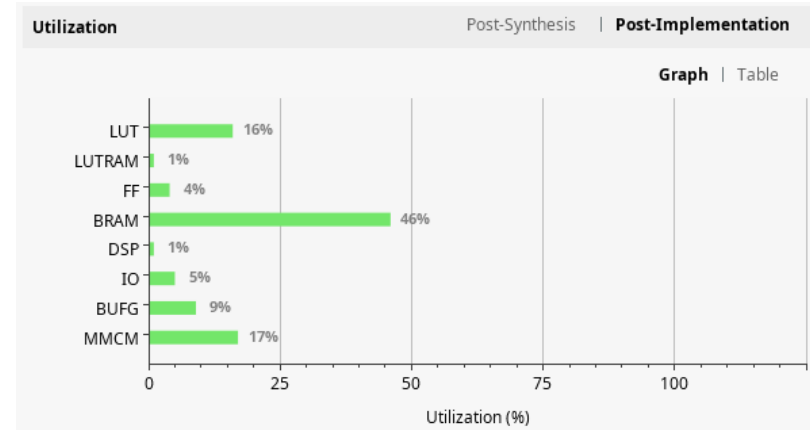


FPGA Implementation Results

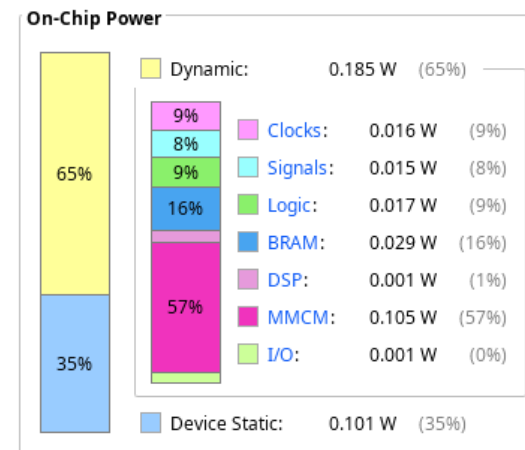
- Implementation on FPGA Arty A7 100T Dev-kit using Xilinx Vivado



Netlist of DN-SoC



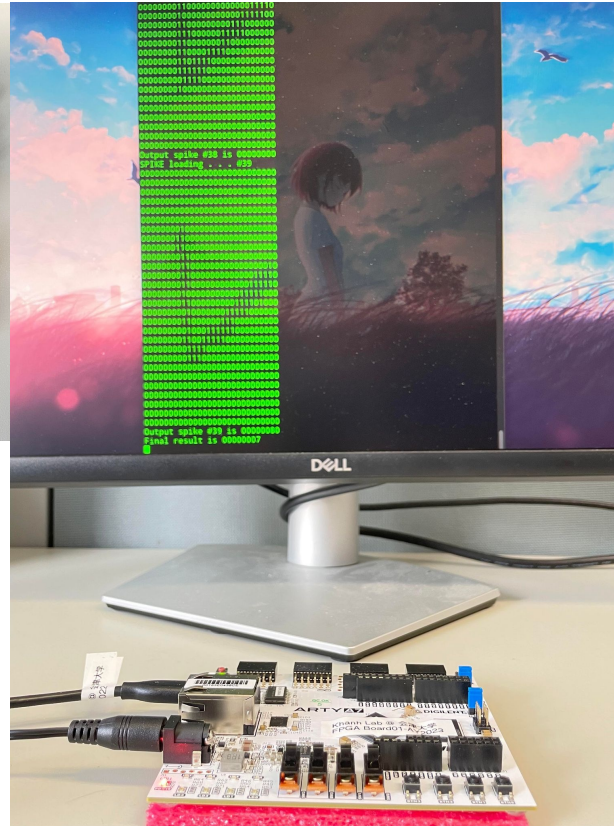
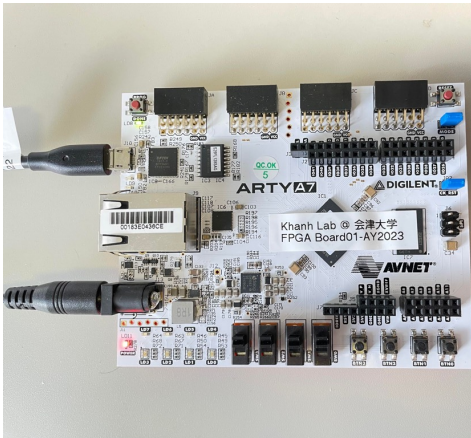
Utilization of DN-SoC



Power consumption of DN-SoC

FPGA Demonstration

- Connection via /dev/ttyUSB1
- UART baud rate = 115200



```

sudo python3 -m serial.tools.miniterm /dev/ttyUSB1 115200

0000000111000000000000000000
00000001100000000000000000
0000000100000000000000001100
000000011000000000000000111110
000000011000000000000000111100
000000010000000000000011111000
0000000110000000001110000000
0000000111000000111110000000
00000001100000011000000000
0000000110000111100000000000
0000000110111100000000000000
0000000111111000000000000000
0000000011110000000000000000
0000000100000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000100000000000000000000
0000000110000000000000000000
0000000110000000000000000010
000000011000000000000011110
0000000110000000000000111110
0000000100000000001111010000
0000000100000000111110000000
0000000110000001110000000000
0000000110000001110000000000
0000000110000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
Output spike #38 is 00000000
SPIKE loading . . . #39
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000100000000000000000000
0000000110000000000000000000
0000000110000000000000000000
0000000110000000000000000010
000000011000000000000011110
0000000110000000000000111110
0000000100000000001111010000
0000000100000000111110000000
0000000110000001110000000000
0000000110000001110000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
0000000000000000000000000000
Output spike #39 is 00000080
Final result is 00000007

```



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**Thank you
for your attention.**