

The Queue Computer Project

QC-1 (QueueCore1) Processing Stage Algorithms

Technical Report, TRQC1PSA03

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1. Fetch Algorithm

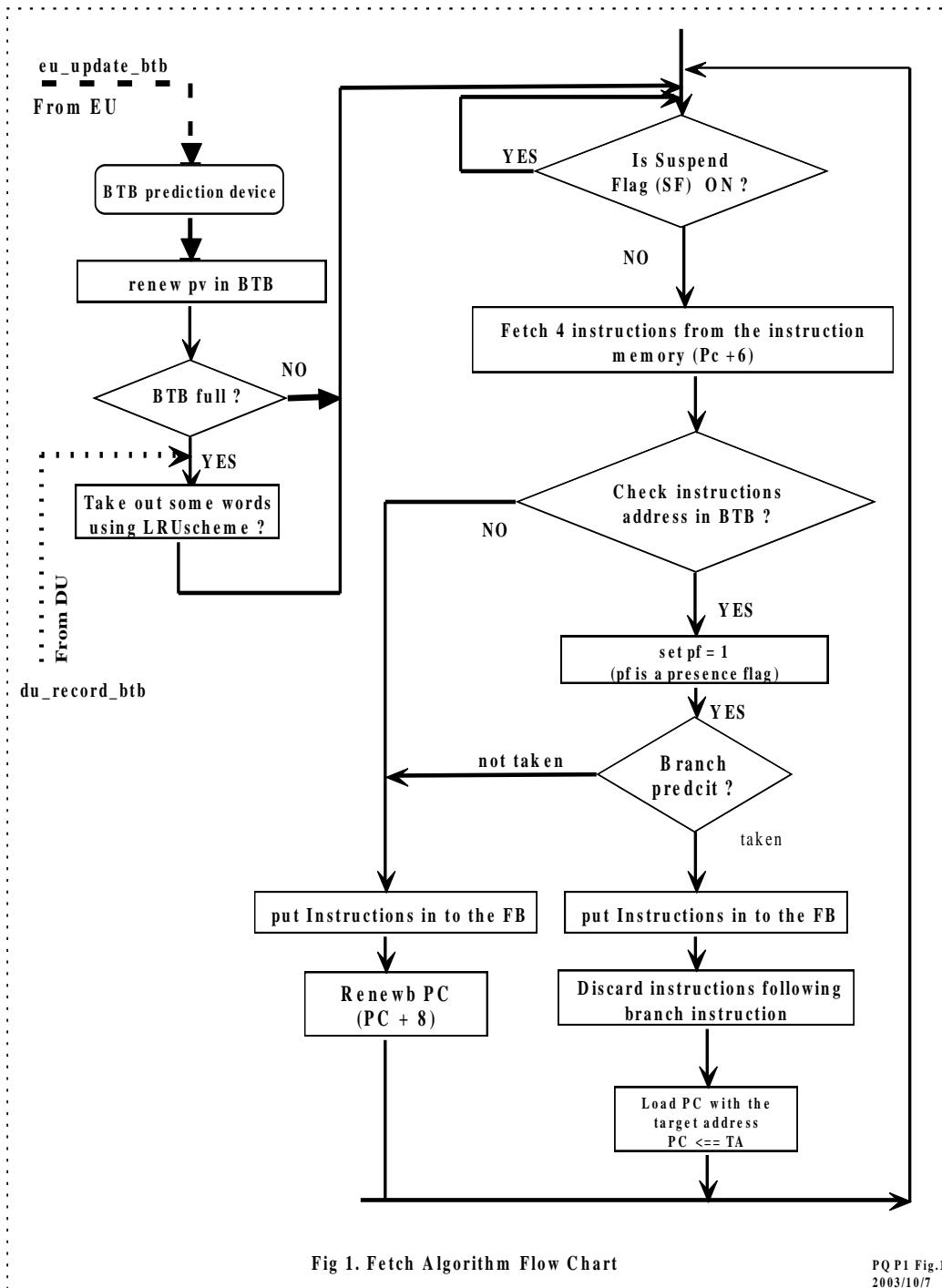
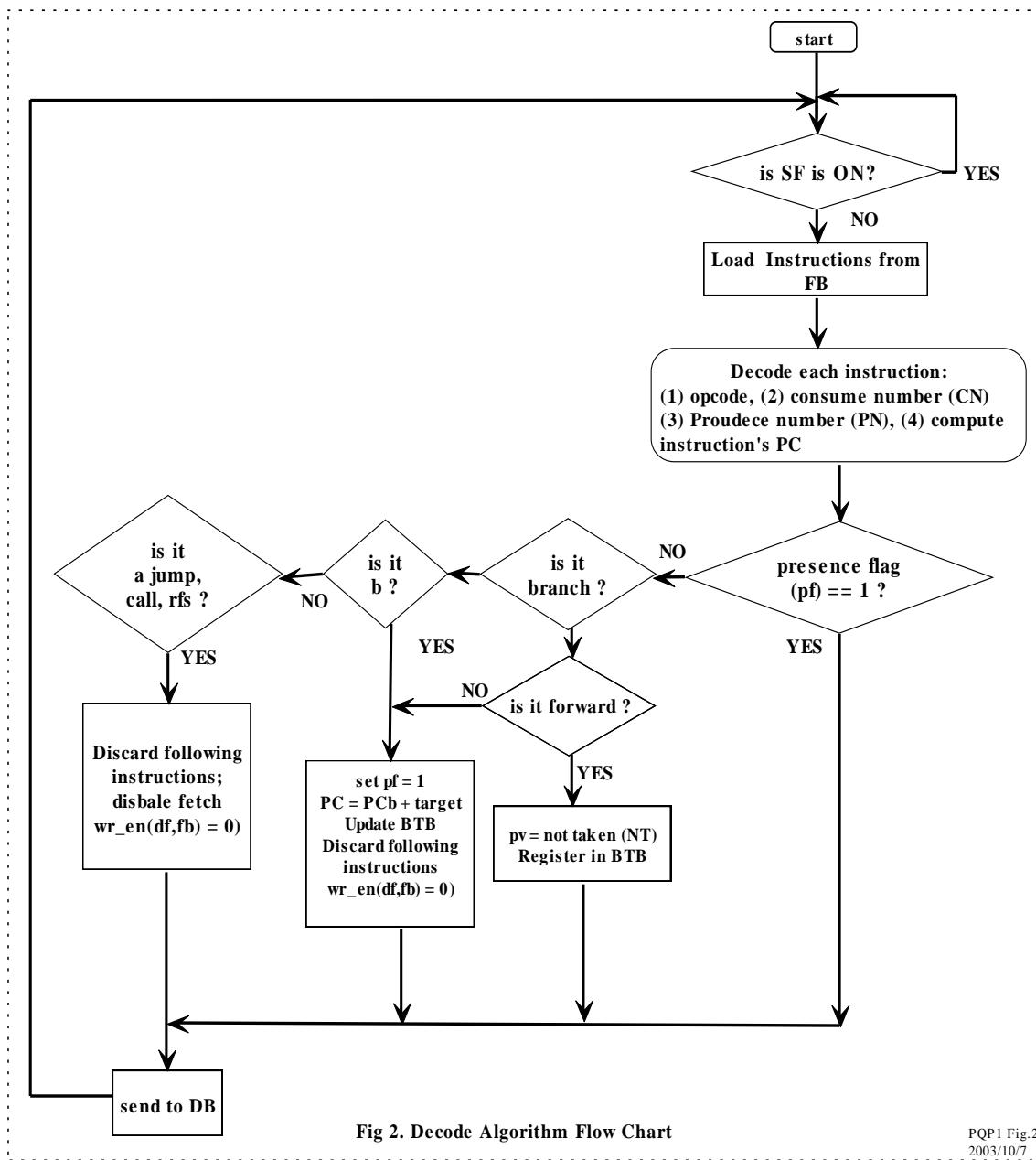


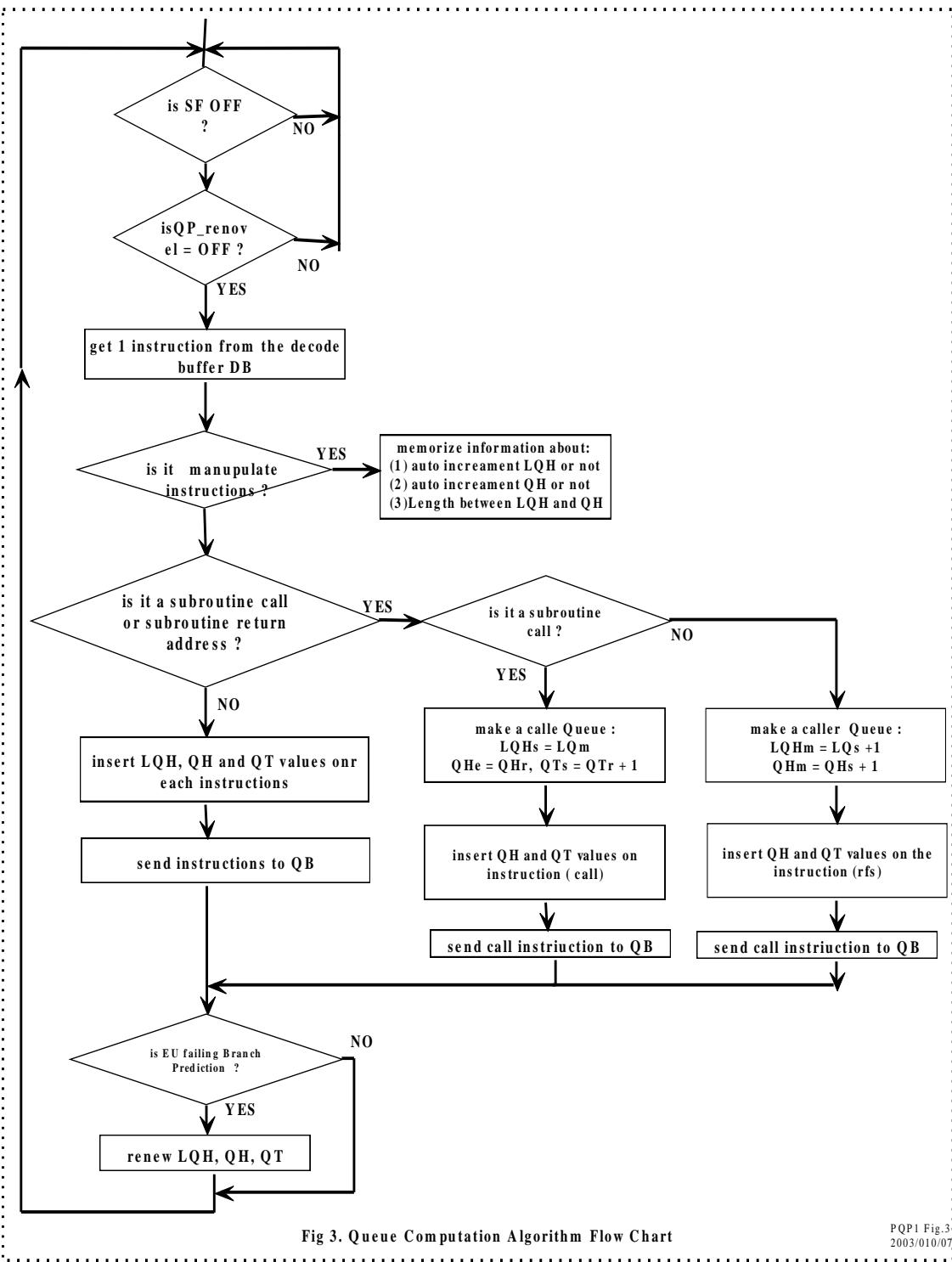
Fig 1. Fetch Algorithm Flow Chart

PQ P1 Fig.1
2003/10/7

2. Decode Algorithm



3. Queue Computation Algorithm (QCU)



4. Barrier and Queue (BQU) Algorithm

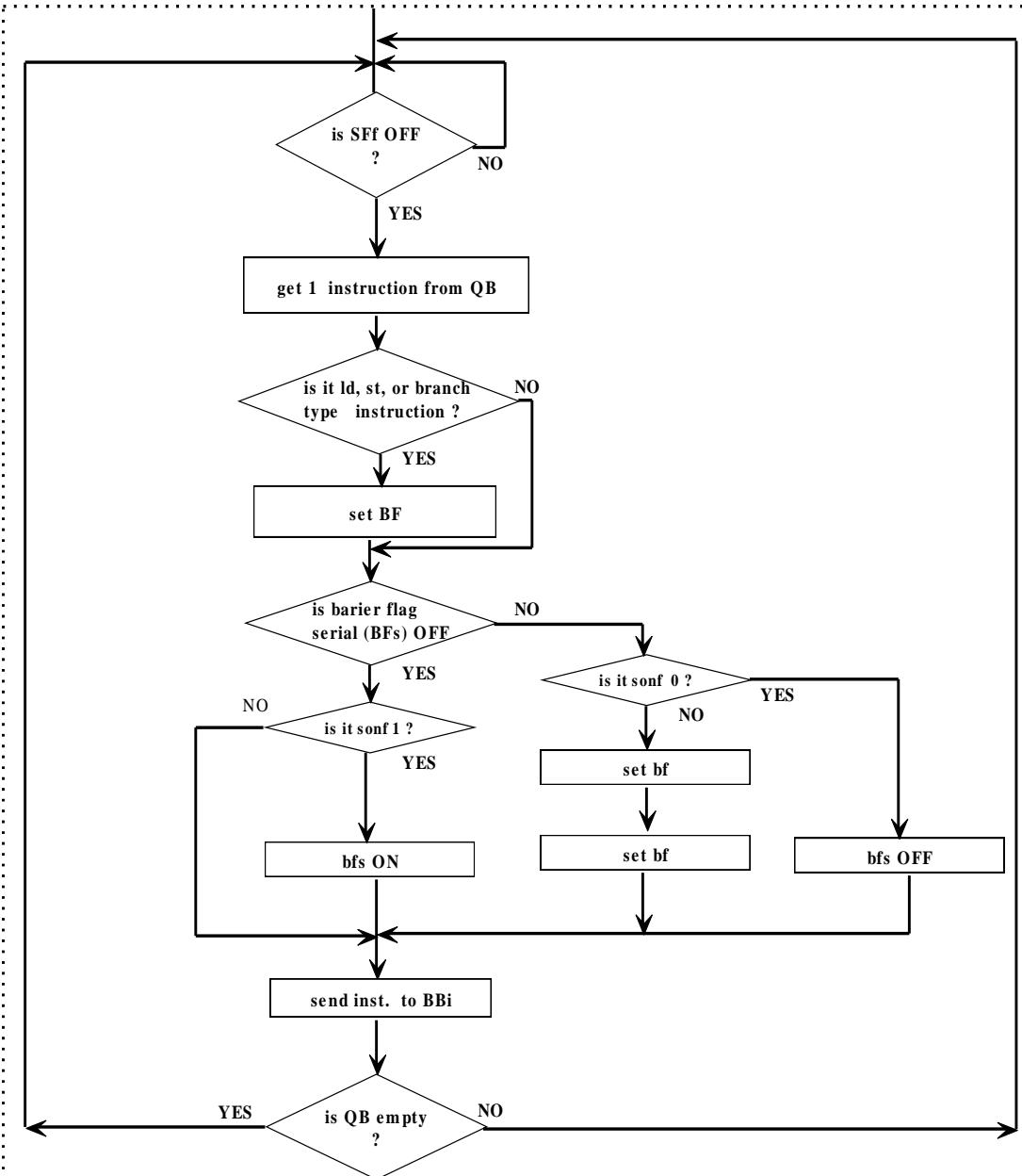


Fig 4. Barriere and Queue Control Algorithm Flow Chart

PQP1 Fig.4
2003/010/07

5. Issue Algorithm

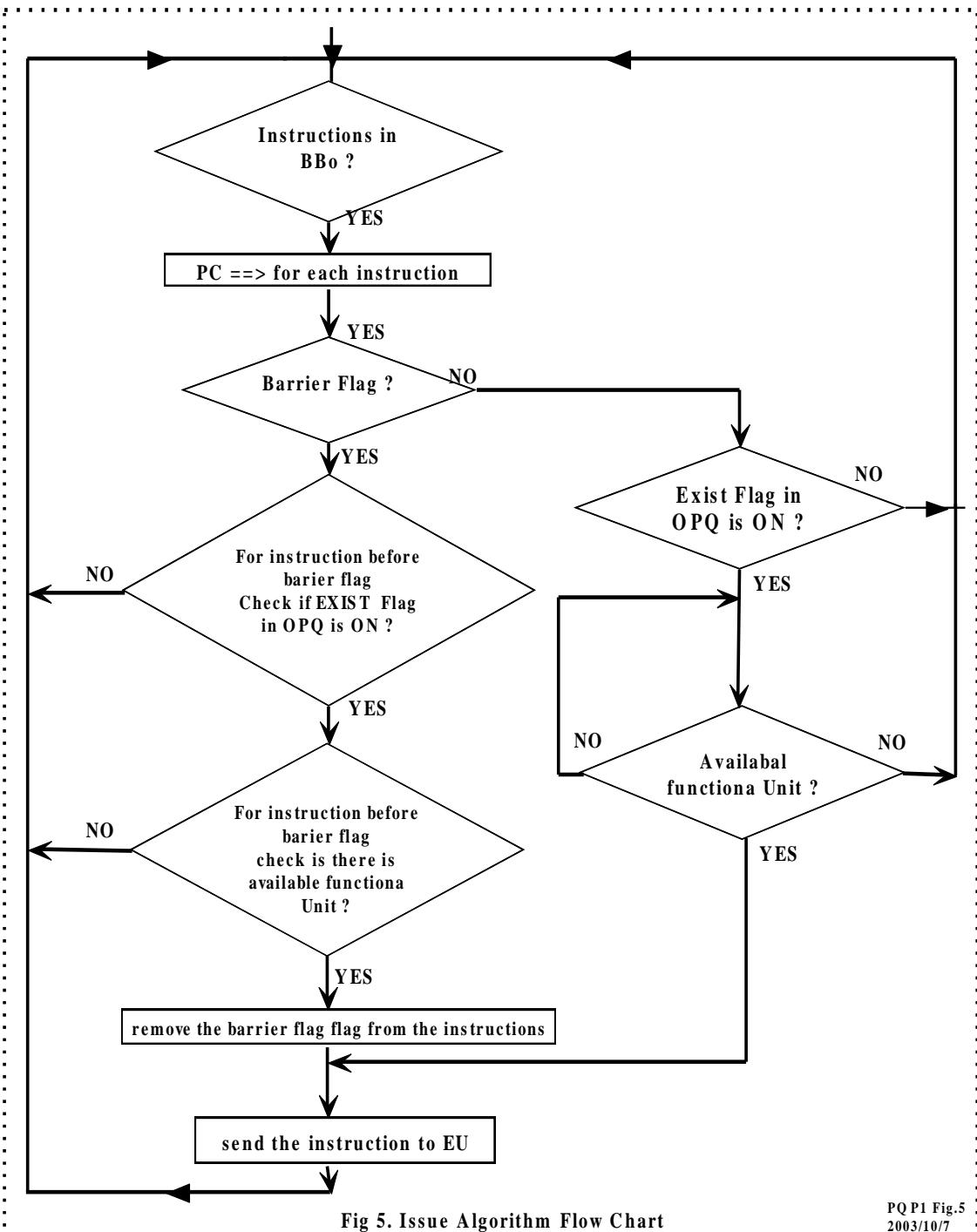


Fig 5. Issue Algorithm Flow Chart

PQ P1 Fig.5
2003/10/7

6. Execution Algorithm

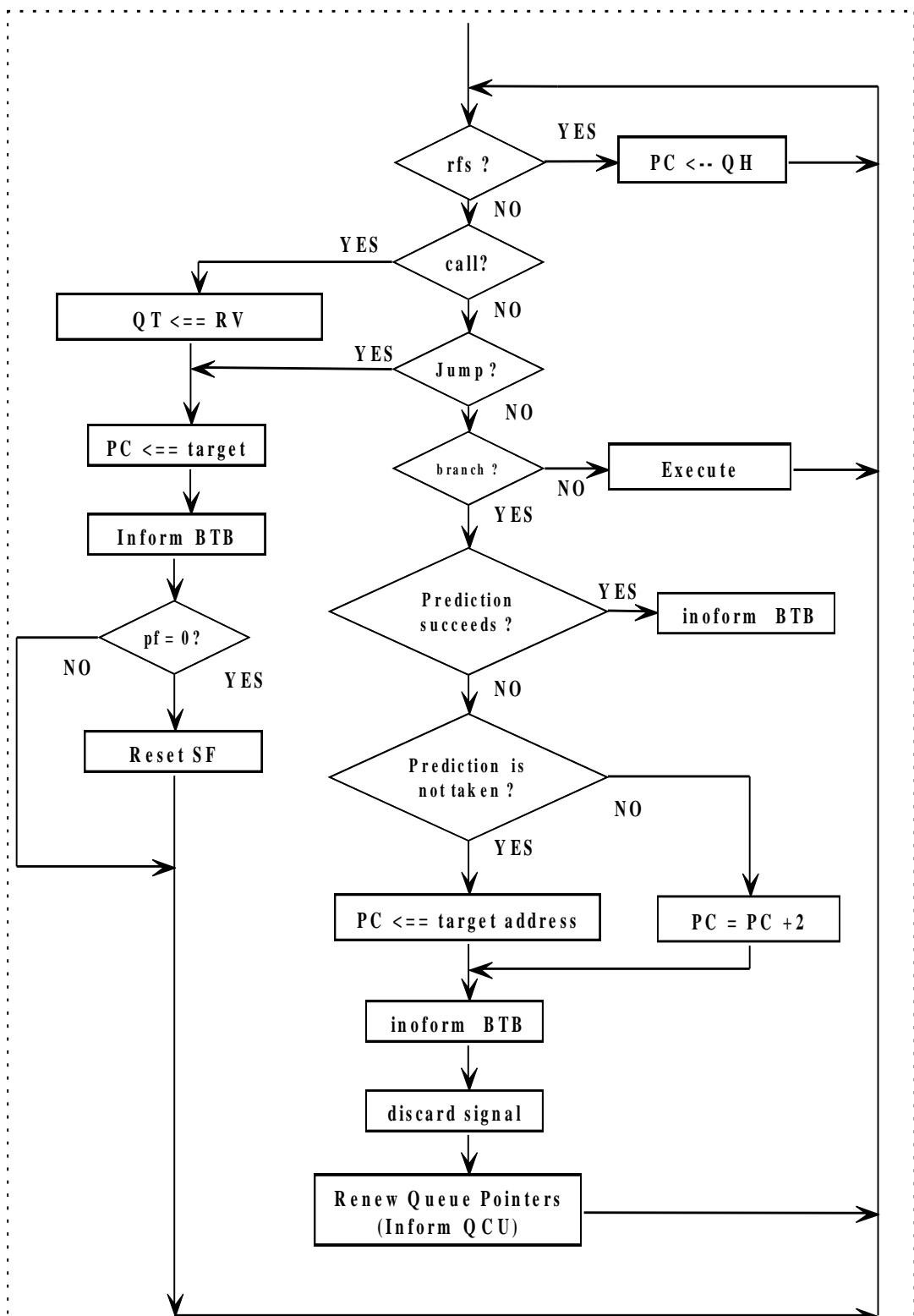


Fig 6. Execution Algorithm Flow Chart

PQP1 Fig.6
2003/010/07

References

1. A. Ben Abdallah, Sotaro Kawata, and M. Sowa, "Design and Architecture for an Embedded 32-bit QueueCore", Journal of Embedded Computing, Special Issue in embedded single-chip multicore architectures, Vol. 2, No. 2, pp. 191-205, 2006.
2. A. Ben Abdallah, T. Yoshinaga, and M. Sowa, "High-Level Modeling and FPGA Prototyping of Produced Order Parallel Queue Processor Core", Journal of supercomputing, Vol. 38, Number 1, pp. 3-15, 2006
3. M. Masuda, A. Ben Abdallah, A. Canedo, "Software and Hardware Design Issues for Low Complexity High-Performance Processor Architecture", The 38th International Conference on Parallel Processing Workshops, pp. 558-565, 2009
4. M. Masuda, A. Canedo, A. Ben Abdallah, "Efficient Code Generation Algorithm for Natural Instruction Level Parallelism-aware Queue Architecture," The 19th Intelligent System Symposium (FAN 2009), pp.308-313, Sep. 2009.(Best Presentation Award).
5. H. Hoshino, A. Ben Abdallah, and K. Kuroda, "Advanced Optimization and Design Issues of a 32-bit Embedded Processor Based on Produced Order Queue Computation Model", IEEE/IFIP Int'l Conf. on Embedded and Ubiquitous Computing (EUC2008),pp.16-22, Dec.2008.
6. A. Canedo, A. Ben Abdallah, and M. Sowa, "Quantitative Evaluation of Common Subexpression Elimination on Queue Machines", Proc. IEEE Int'l Sym. on Parallel Architectures, Algorithms, and Networks (I-SPAN 2008), pp.25-30. 2008.
7. A. Canedo, A. Ben Abdallah, and M. Sowa, "Queue Register File Optimization Algorithm for QueueCore Processor", Proc. IEEE 19th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2007), pp. 169-176, 2007.
8. A. Canedo,A. Ben Abdallah, and M. Sowa, "An Efficient Code Generation Algorithm for Code Size Reduction using 1-offset P-Code Queue Computation Model", Proc. IFIP International Conference on Embedded and Ubiquitous Computing (EUC07), pp. 196-208, 2007
9. A. Canedo, A. Ben Abdallah, and M. Sowa, "Compiler Framework for an Embedded 32-bit Queue Processor" , Proc. of the International Conference on Convergence Information Technology (ICCIT07), Gyeongju, South Korea, pp. 877-884, 2007.

10. A. Ben Abdallah, T. Yoshinaga, and M. Sowa, "High-Level Modeling and FPGA Prototyping of Produced Order Parallel Queue Processor Core", Journal of supercomputing, Vol. 38, Number 1, pp. 3-15, 2006.
11. A. Ben Abdallah, Sotaro Kawata, and M. Sowa, "Design and Architecture for an Embedded 32-bit QueueCore", Journal of Embedded Computing, Special Issue in embedded single-chip multicore architectures, Vol. 2, No. 2, pp. 191-205, 2006.
12. M. Sowa, A. Ben Abdallah, and T. Yoshinaga, "Processor Architecture Based on Produced Order Computation Model", "Journal of Supercomputing, Vol. 32, No. 3, pp. 217-229, June 2005.
13. A. Ben Abdallah, M. Arsenji, S. Shigeta, T. Yoshinaga, and M. Sowa, "Modular Design Structure and High-Level Prototyping for Novel Embedded Processor Core", Proc. of International Conference on Embedded and Ubiquitous Computing (EUC2005), LNCS Vol.3824, pp. 340-349, 2005.
14. A. Ben Abdallah, M. Arsenji, K. Kiuchi, M. Akanda, S. Shigeta, T. Yoshinaga, and M. Sowa, "PQPpfB: Parallel Queue Processor Architecture in Verilog-HDL", Proc. of 66th Information Processing Society of Japan, pp. 3F-4, March 2004.
15. A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "Architectural Issues in the Design of a High Performance Parallel Queue Processor", Proc. of 4th Tunisia-Japan Symposium on Science and Technology (TJASSST2003), April 2003.
16. A. Ben Abdallah, S. Shigeta, T. Yoshinaga, and M. Sowa, "Reduced Bit-Width Instruction Set Architecture for Q-mode Execution in Hybrid Processor Architecture (FaRM-rq)", Proc. of Information Processing Society of Japan, pp. 19-23, June 2003.
17. A. Ben Abdallah, K. Nikolova, and M. Sowa, "FARM-Queue Mode: On a Practical Queue Execution Model", Proc. of the Int. Conf. on Circuits and Systems, Computers and Communications, pp.939-944, July 2001.
18. A. Ben Abdallah, K. Nikolova T. Yoshinaga, and M. Sowa, "FARM QUEUE MODE: On a Practical Queue Execution Model (QEM)", TIWSS'01, October 2001.
19. A. Ben Abdallah, K. Nikolova, and M. Sowa, "FARM-Queue Execution Model: Towards an Alternative Computing Paradigm", Proc. of IPSJ Symposium, Yokohama pp.99-100, March 2000.
20. A. Ben Abdallah, M. Sarem., and M. Sowa, "Acyclic DFG on a Queue Machine", Proc. of JSPP, Tokyo, pp.119-120, 2000.
21. A. Ben Abdallah, and M. Sowa, "DRA: Dynamic Register Allocator Mechanism for FaRM Microprocessor", Proc. of the 3rd International Workshop on Advanced Parallel Processing Technologies (APPT'99), pp.131-136, Oct.1999.

22. Hiroki Hoshino, Abderazek Ben Abdallah and Kenichi Kuroda. Advanced Optimization and Design Issues of a 32-bit Embedded Processor Based on Produced Order Queue Computation Model, IEEE/IFIP International Conference on Embedded and Ubiquitous Computing, Shanghai, pp.16-22, Dec. 2008.
23. A. Ben Abdallah, et. all "Modular Design Structure and High-Level Prototyping for Novel Embedded Processor Core", International Conference on Embedded and Ubiquitous Computing (EUC2005), LNCS Vol.3824, pp. 340-349, 2005
24. A. Ben Abdallah, et. all,"Queue Processor for Novel Queue Computing Paradigm Based on Produced Order Scheme", IEEE computer Society, Proc. of the The 7th High Perfomance Computing and Grid in Asia Pacific Region (HPCAsia2004), pp. 169-177, July 2004