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PHENIC:
Photonics Network-on-Chip
Design Flow

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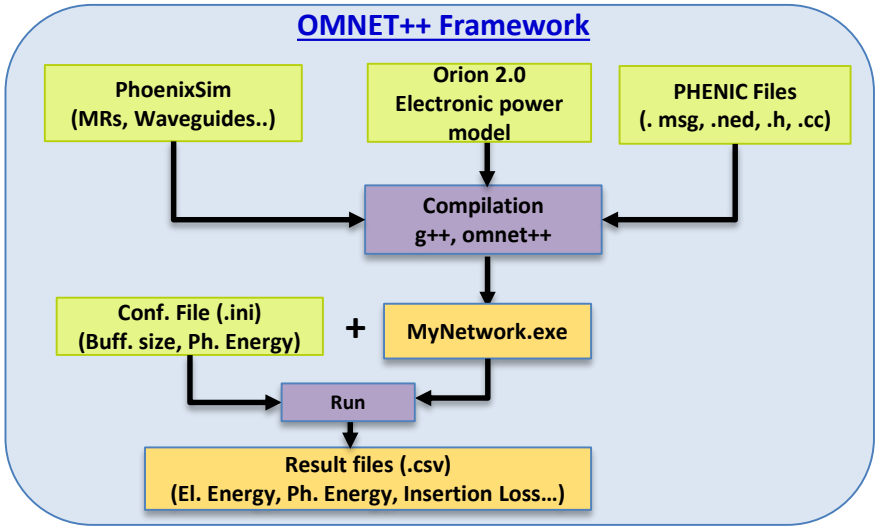
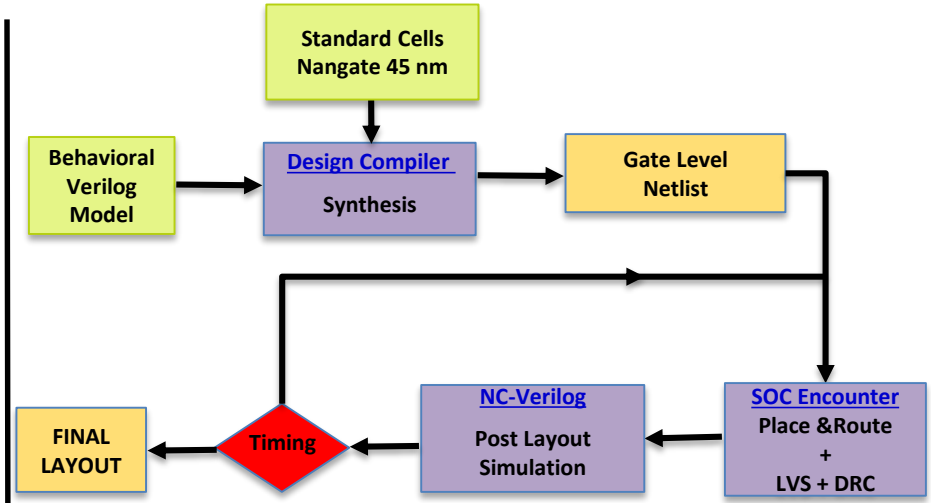
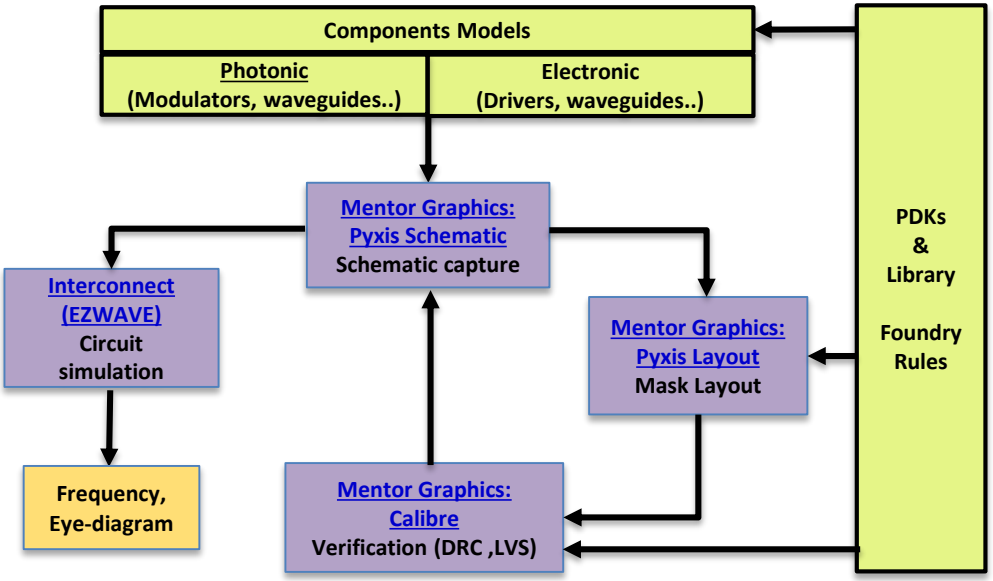
PHENIC Design Flow



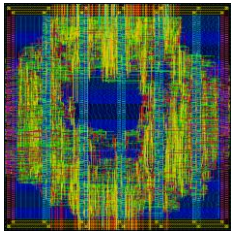
PHENIC SW Design Flow



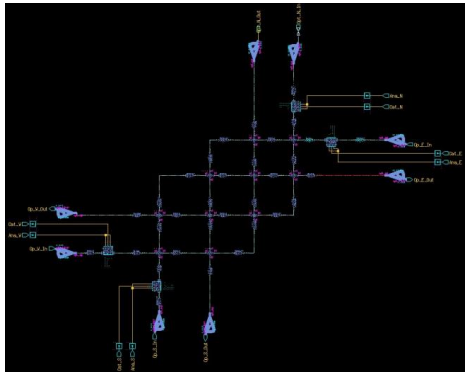
Si-ECN Design Flow



PHENIC HW Design Flow



PHENIC's electronic controller layout in 45 nm process



Part of PHENIC's photonic switch Passive Routing

PHENIC Design Flow

Configuration parameters

Process technology	32 nm
Number of tiles	64/256
Chip area (equally divided among tiles)	400 mm^2
Core frequency	2.5 GHz
Electronic Control frequency	5 GHz
Buffer depth	2
Message size	2 KB

Delay Contribution for 32nm Technology Nodes.

Modulator Driver	16.3 ps
Modulator	20 ps
Detector TIA	6.9 ps
Detector	0.3 ps
Waveguide propagation	46.7 ps/cm
Electronic Wire propagation	200 ps/cm
Router delay	600 ps (3 clock cycles)

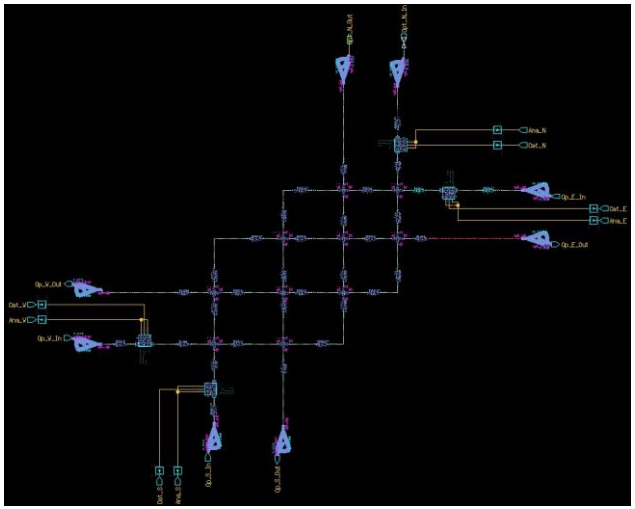
Insertion loss parameters

Parameter	Value
Propagation loss (silicon)	1.2 dB/cm
Waveguide crossing	0.12 dB
Waveguide bending	0.005 dB/90°
Drop into a ring	0.5 dB
Passing by a ring	0.005 dB

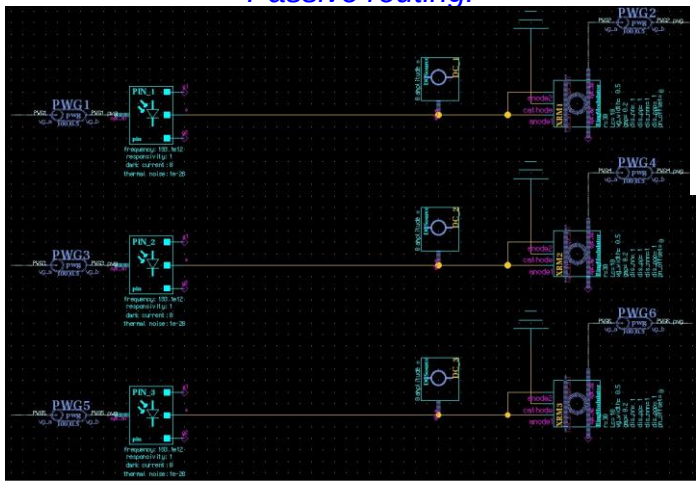
Energy Contribution for 32nm Technology Nodes.

Buffering	0.12 pJ/bit
Electronic Crossbar	0.36 pJ/bit
Electronic Wire	o.34 pJ/mm/bit
Electronic Static	0.35 pJ/bit
Modulator Driver	0.32 pJ/bit
Modulator	0.025 pJ/bit
Detector TIA	0.69 pJ/bit
Detector	0.05 pJ/bit
Micro-Ring ON/OFF	0.375
Micro-Ring Static Thermal Tuning	1 μW/Ring/K

HW Design Results



Part of PHENIC's photonic switch. Passive routing.



Wavelength-shifting controller.
Three required channels at each port for a network configuration of 4x4.

+52% Xbr, +38 % Torus
+76 % Blocking networks

	PHENIC	PHENIC_BL	Chan_Mesh	Chan_Xb	Shacham
Mod/Detc	64	64	64	64	64
Switch	1152	852	768	1152	1620
ACKs	640	–	–	–	–
Total	1856	916	832	1216	1684
Static thermal tuning (mW)	37	18	16	24	33

(a)

	PHENIC	PHENIC_BL	Chan_Mesh	Chan_Xb	Shacham
Mod/Detc	256	256	256	256	256
Switch	4608	3252	3072	4608	6324
ACKs	2560	–	–	–	–
Total	7424	3508	3328	4864	6580
Static thermal tuning (mW)	149	71	67	98	131

(b)

Micro-ring requirement. (a) 64 cores, (b) 256 cores

Architecture	Area (um^2)		Power (uW)	
PHENIC	18130		210	
Baseline *[oasis]*	28306	-35%	311	-32%

Electronic controller hardware complexity evaluation results after optimization.