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# OASIS 3D Fault Tolerant Router Hardware Physical Design with TSV OASIS-3DFTRV1

## Technical Report

© [Adaptive Systems Laboratory](#)  
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# IMPORTANT NOTES

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- This tutorial focuses mainly on the integration of TSV with 3D-OASIS-NoC router.
- It covers the TSV creation, synthesis, place and route, and LVS and DRC check.
- Post layout simulation and pad insertion steps are not included.
- Complete details about the execution of these two steps can be found in the previously made technical report [**Ref.1**].



# TSV Physical Design Steps

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1. Environment
2. TSV layout
3. Modify lef file
4. Place & Route
5. ACKNOWLEDGEMENT



# Objectives

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- After completing this tutorial you will be able to:
  1. Design TSV layout using Virtuoso
  2. Synthesize 3D-OASIS-NoC (3D-ONoC) router with TSV using Design-Compiler CAD tool
  3. Place & Route (P&R) 3D-ONoC router with TSV using Cadence SoC-Encounter
  4. Learn how to make TSV layout, the synthesis and P&R via:
    - The CAD Graphic User Interface
    - Tcl script



# Prerequisite

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- Understand the previously made “OASIS 3D-Router Hardware Physical Design” technical report [Ref.1].
- Study 3D-OASIS-NoC architecture and its main components [Ref.2].
- Read the Manual and Release Notes of the FreePDK3D45 design tool kit [Ref.3] and understand the aspects of the used TSV component.



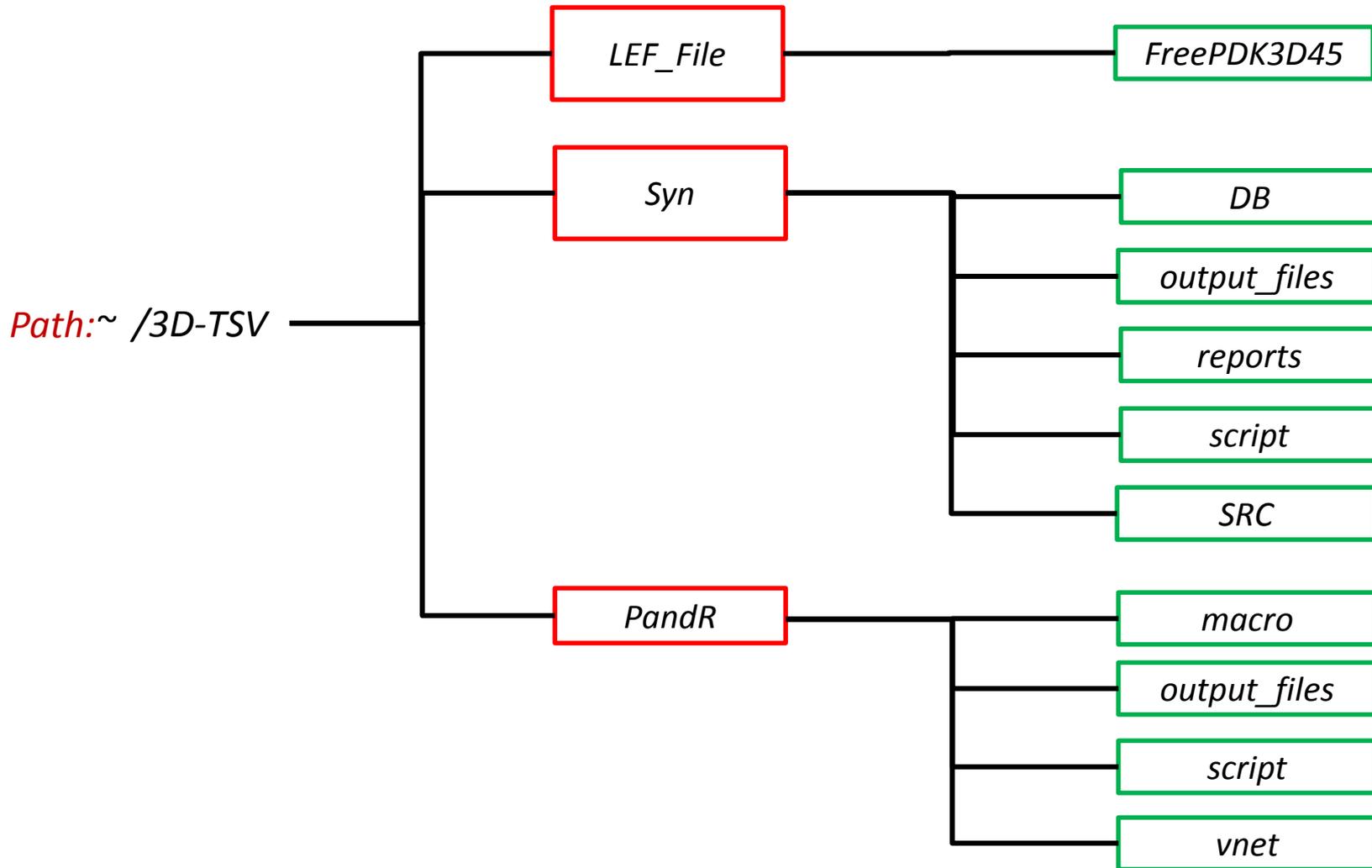
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# 1. Environment



# Tutorial directory structure





# Environment: FreePDK3D45

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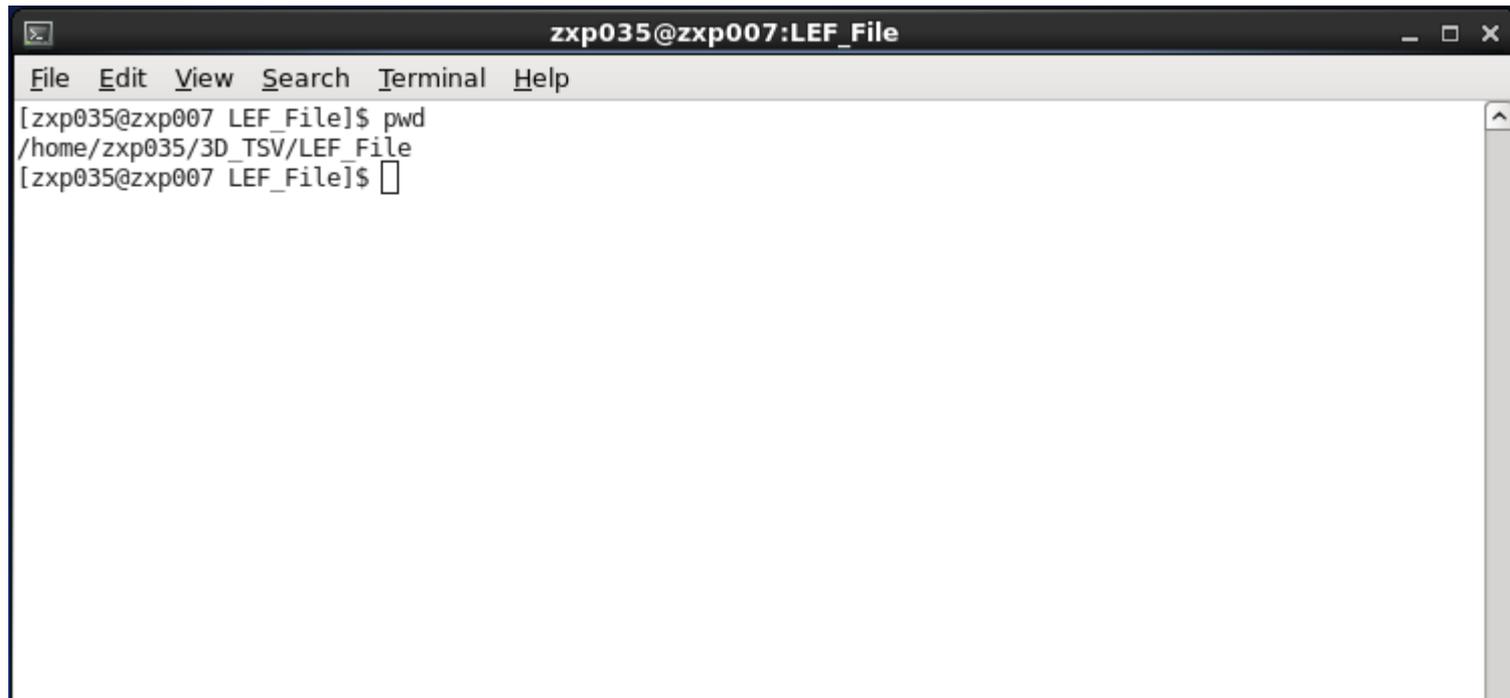
- The Process Design Kit used in this tutorials are obtained from NCSU FreePDK3D45.
- Go to: [http://www.eda.ncsu.edu/eda\\_registration.php](http://www.eda.ncsu.edu/eda_registration.php)
- Verification is required so enter your email address.
- You will receive an email with a link to download FreePDK3D45.
- Extract the downloaded archive and copy the *FreePDK3D45* folder in your working directory:

***/home/zxp035/3D-TSV/LEF\_File***



# Environment: Setup

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A terminal window titled 'zxp035@zxp007:LEF\_File' with a menu bar (File, Edit, View, Search, Terminal, Help). The terminal shows the command 'pwd' being executed, resulting in the output '/home/zxp035/3D\_TSV/LEF\_File'.

```
zxp035@zxp007:LEF_File
File Edit View Search Terminal Help
[zxp035@zxp007 LEF_File]$ pwd
/home/zxp035/3D_TSV/LEF_File
[zxp035@zxp007 LEF_File]$
```

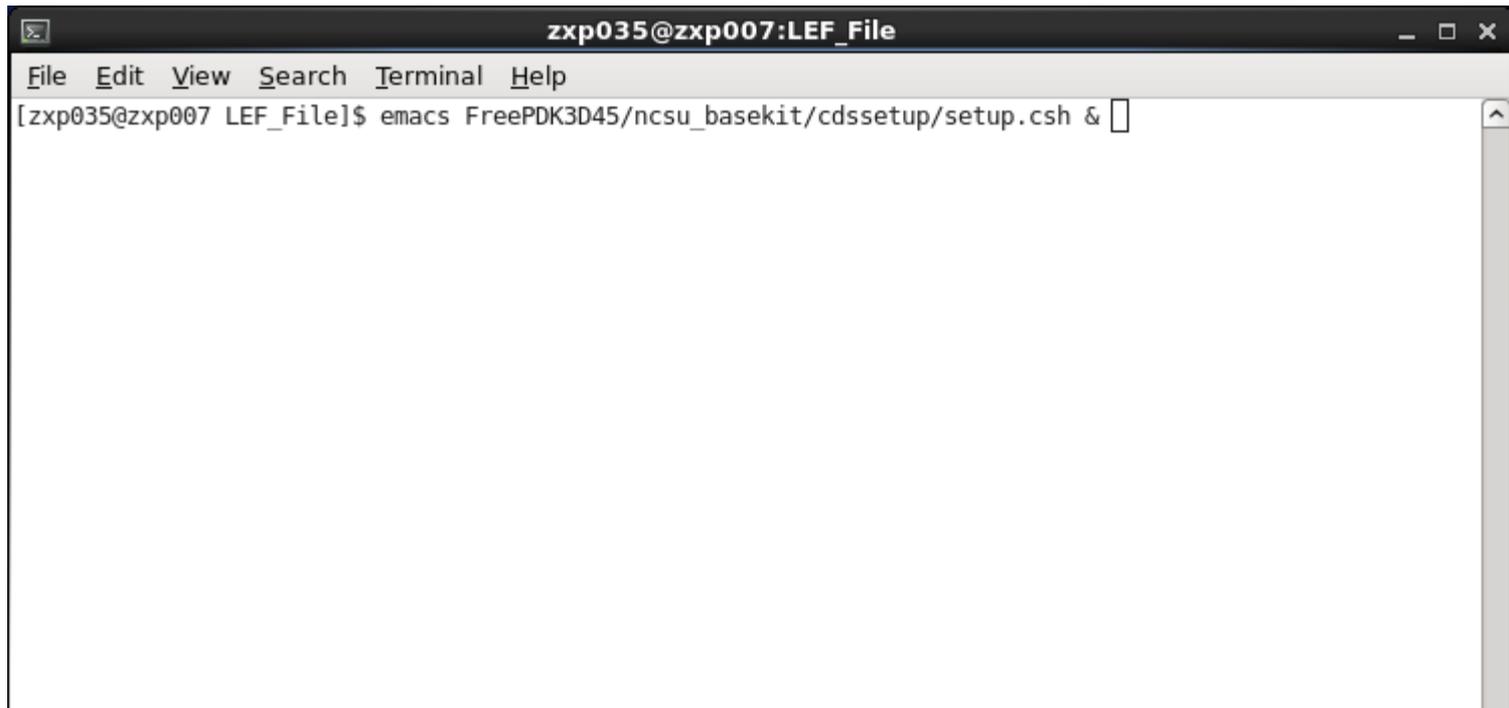
---

Go to ***/home/zxp035/3D-TSV/LEF\_File*** where the TSV folder is located



# Environment: Setup

---

A terminal window titled 'zxp035@zxp007:LEF\_File' with a menu bar (File, Edit, View, Search, Terminal, Help). The command prompt shows the execution of 'emacs FreePDK3D45/ncsu\_basekit/cdssetup/setup.csh &' with a cursor at the end of the line.

```
zxp035@zxp007:LEF_File
File Edit View Search Terminal Help
[zxp035@zxp007 LEF_File]$ emacs FreePDK3D45/ncsu_basekit/cdssetup/setup.csh & █
```

---

Type **emacs FreePDK3D45/ncsu\_basekit/cdssetup/setup.csh &**



# Environment: Setup

```
emacs@zxp007.u-aizu.ac.jp (on zxp007.u-aizu.ac.jp)
File Edit Options Buffers Tools Sh-Script Help
#####
#
# FreePDK Setup Script
# 2/23/2008 by Rhett Davis (rhett_davis@ncsu.edu)
#
#####

# Set the PDK DIR variable to the root directory of the FreePDK distribution
setenv PDK_DIR /local/home/wdavis/fp3d/FreePDK3D45
# Set CDSHOME to the root directory of the Cadence ICOA installatio
setenv CDSHOME /afs/eos/dist/cadence2008/ic

if !(-f ${PWD}/.cdsinit) # Set the PDK_DIR variable to the root directory of the FreePDK distribution
cp ${PDK_DIR}/ncsu_basekit/cdssetup/cds.lib ${PWD}/.cdsinit
endif setenv PDK_DIR /home/zxp035/3D_TSV/LEF_File/FreePDK3D45
# Set CDSHOME to the root directory of the Cadence ICOA installatio
setenv CDSHOME /opt/vdec/Cadence/IC_06.15.011

if !(-f ${PWD}/cds.lib)
cp ${PDK_DIR}/ncsu_basekit/cdssetup/cds.lib ${PWD}/cds.lib
endif
```

Change the following paths to link to the FreePDK3D45 libraries:

- /local/home/wdavis/fp3d/FreePDK3D45 → /home/zxp035/3D\_TSV/LEF\_File/FreePDK3D45
- /afs/eos/dist/cadence2008/ic → /opt/vdec/Cadence/IC\_06.15.011



# Environment: Setup

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A screenshot of a terminal window. The title bar reads 'zxp035@zxp007:LEF\_File'. The menu bar includes 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows '[zxp035@zxp007 LEF\_File]\$ tcsh' with a cursor at the end of the line. The terminal area is mostly empty, with a vertical scrollbar on the right side.

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Initially *bash* will start, so type “**tcsh**” to start cshr



# Environment: Setup

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A terminal window titled 'zxp035@zxp007:LEF\_File' with a menu bar containing 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows the command 'source FreePDK3D45/ncsu\_basekit/cdssetup/setup.csh' being entered.

```
zxp035@zxp007:LEF_File  
File Edit View Search Terminal Help  
[zxp035@zxp007 LEF_File]$ source FreePDK3D45/ncsu_basekit/cdssetup/setup.csh
```

---

Type **source FreePDK3D45/ncsu\_basekit/cdssetup/setup.csh**



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## 2. TSV Layout



# Virtuoso: TSV layout steps

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A screenshot of a terminal window titled 'zxp035@zxp007:LEF\_File'. The window has a menu bar with 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows '[zxp035@zxp007 LEF\_File]\$ virtuoso &' with a cursor at the end of the command. The terminal area is mostly empty, indicating the command has been entered but not yet executed or the output is not visible.

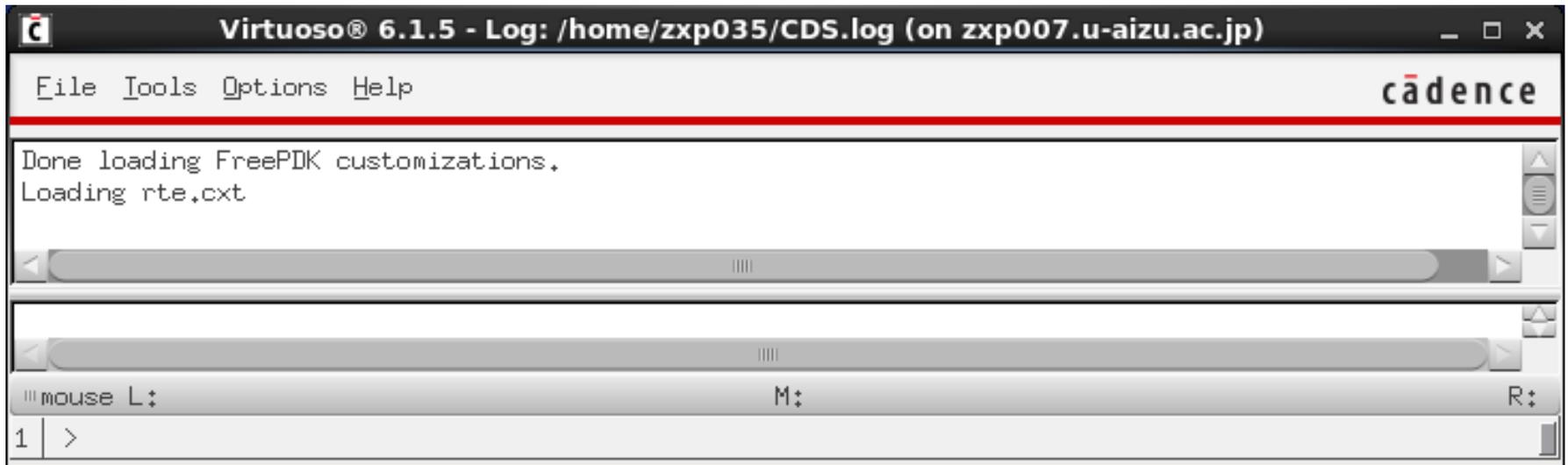
```
zxp035@zxp007:LEF_File
File Edit View Search Terminal Help
[zxp035@zxp007 LEF_File]$ virtuoso &
```

---

Type **virtuoso&** to start Virtuoso



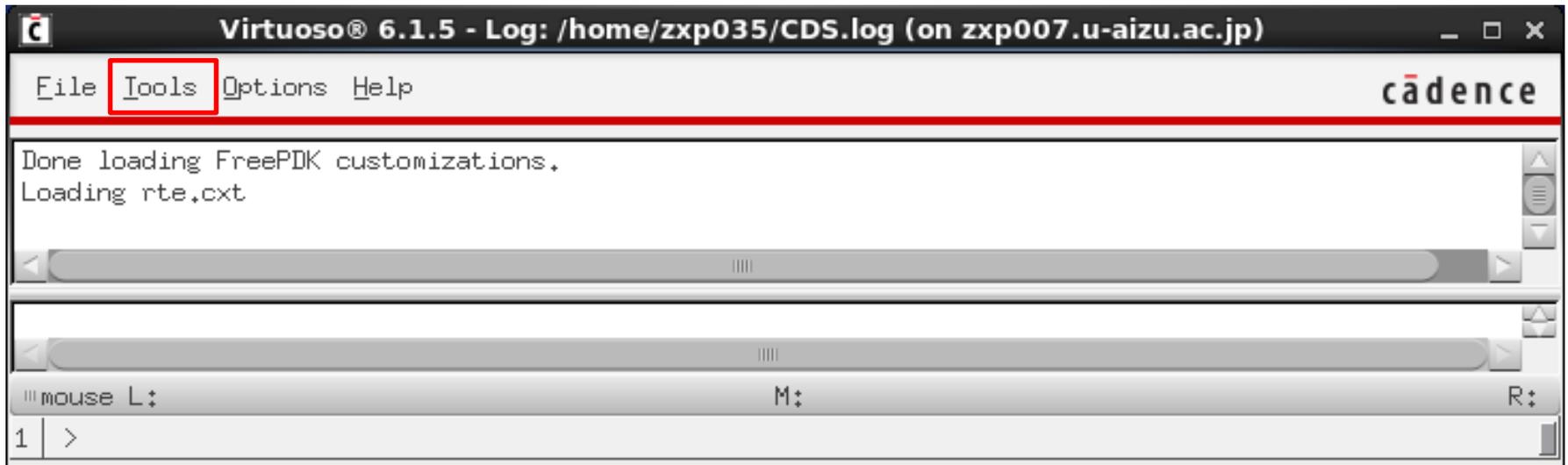
# Virtuoso: TSV layout steps





# Virtuoso: TSV layout steps

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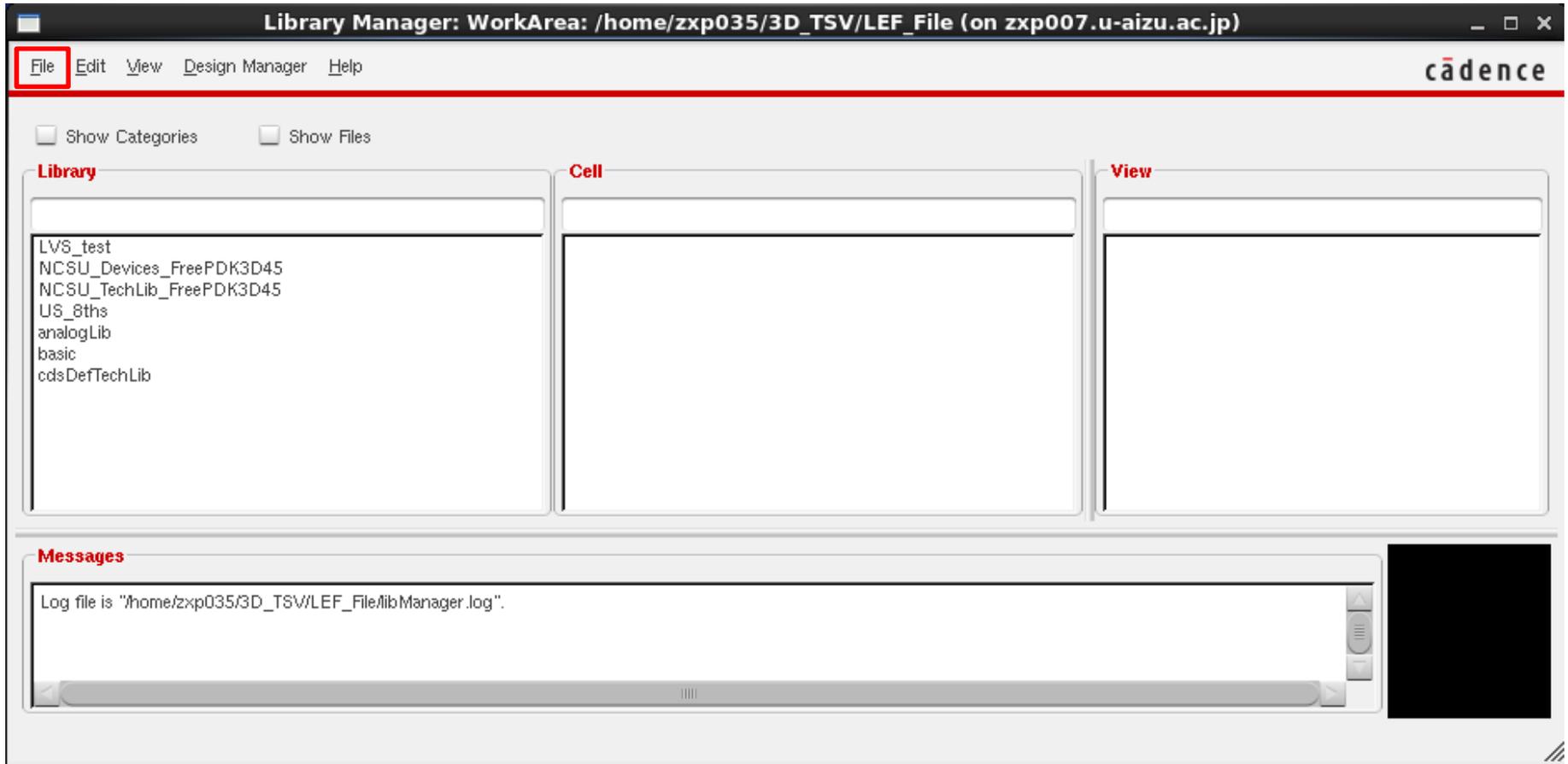


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First, we should create a library.  
Click **Tools->Library Manager**



# Step1: Create library



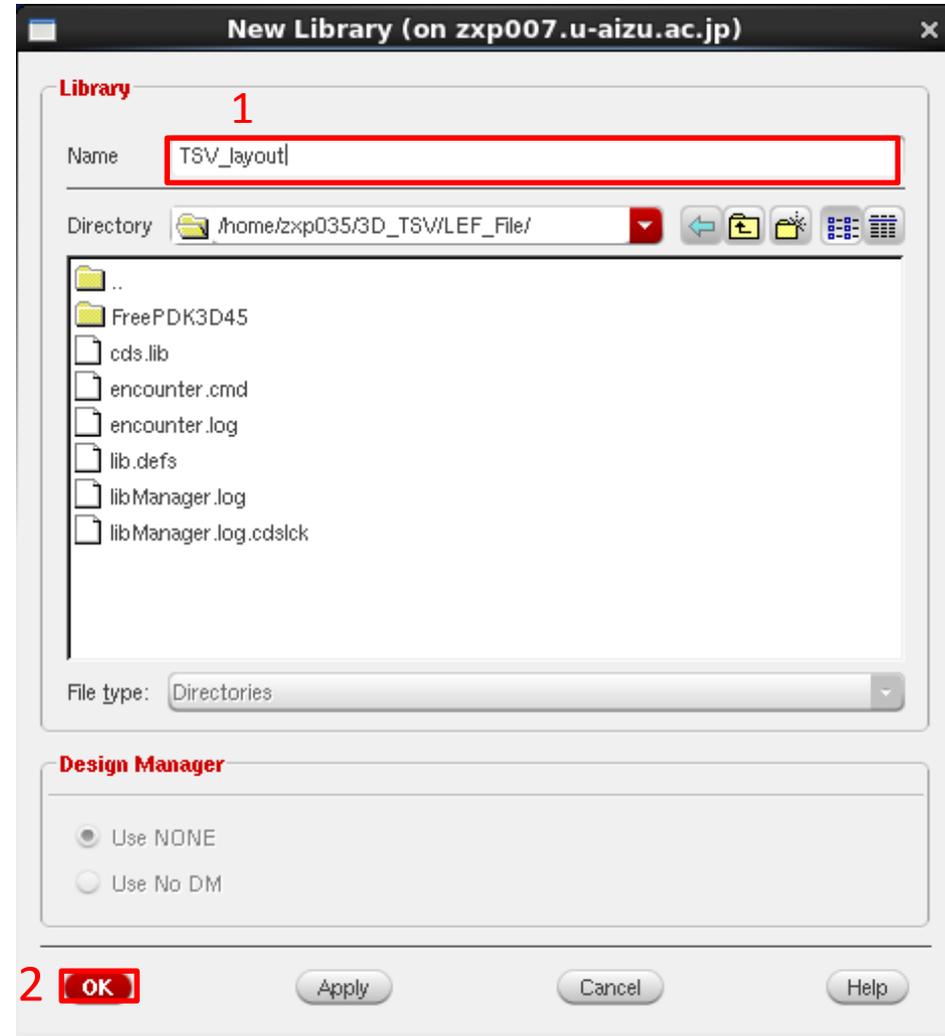
Click File -> New -> Library



# Step1: Create library

## a- Library name

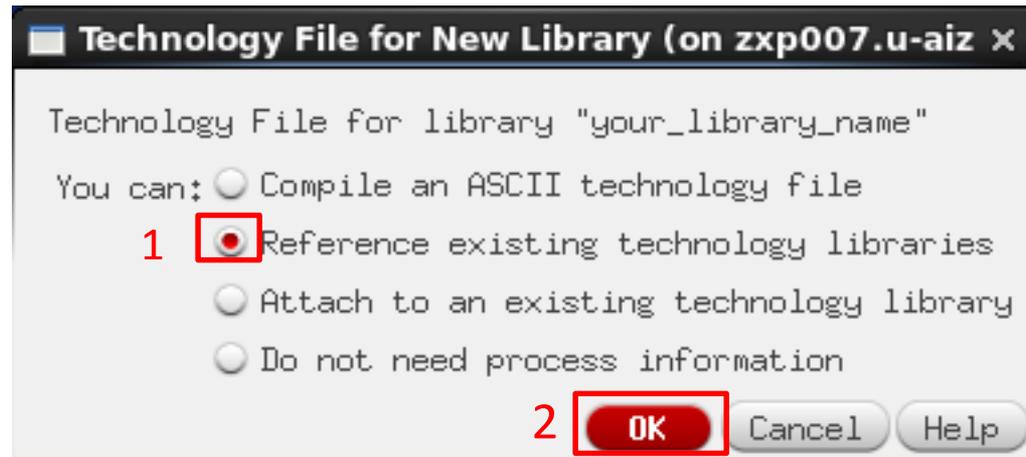
1. In *Library Name*, type **TSV\_layout**
2. Click **OK**





# Step1: Create library b- Technology file

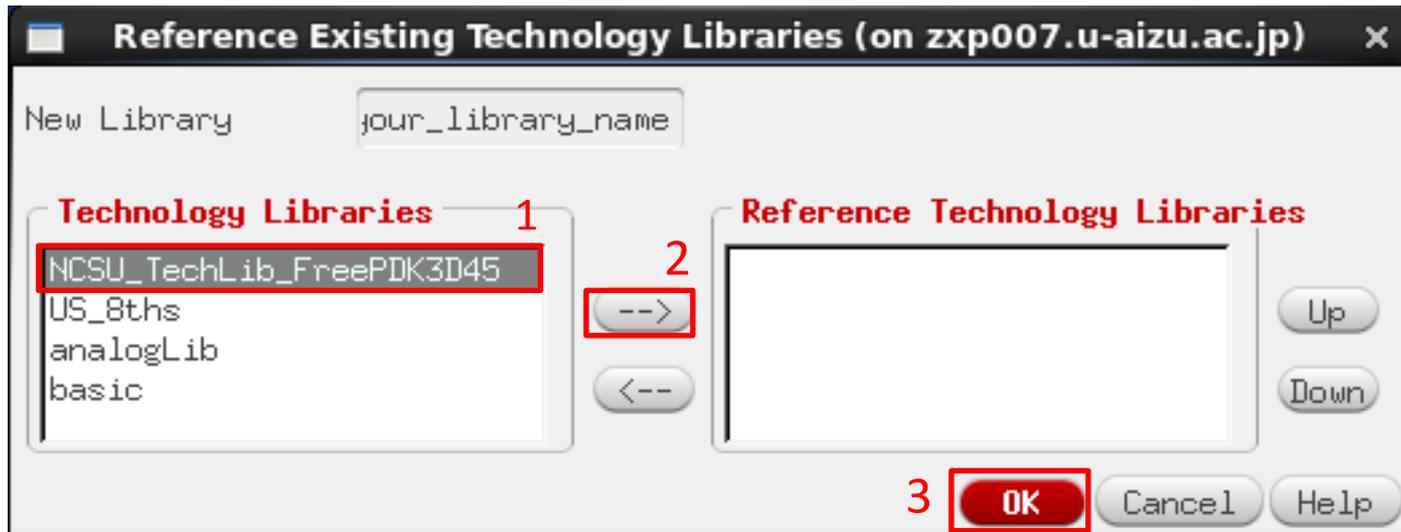
---



1. Check **Reference existing technology libraries**
2. Click **OK**



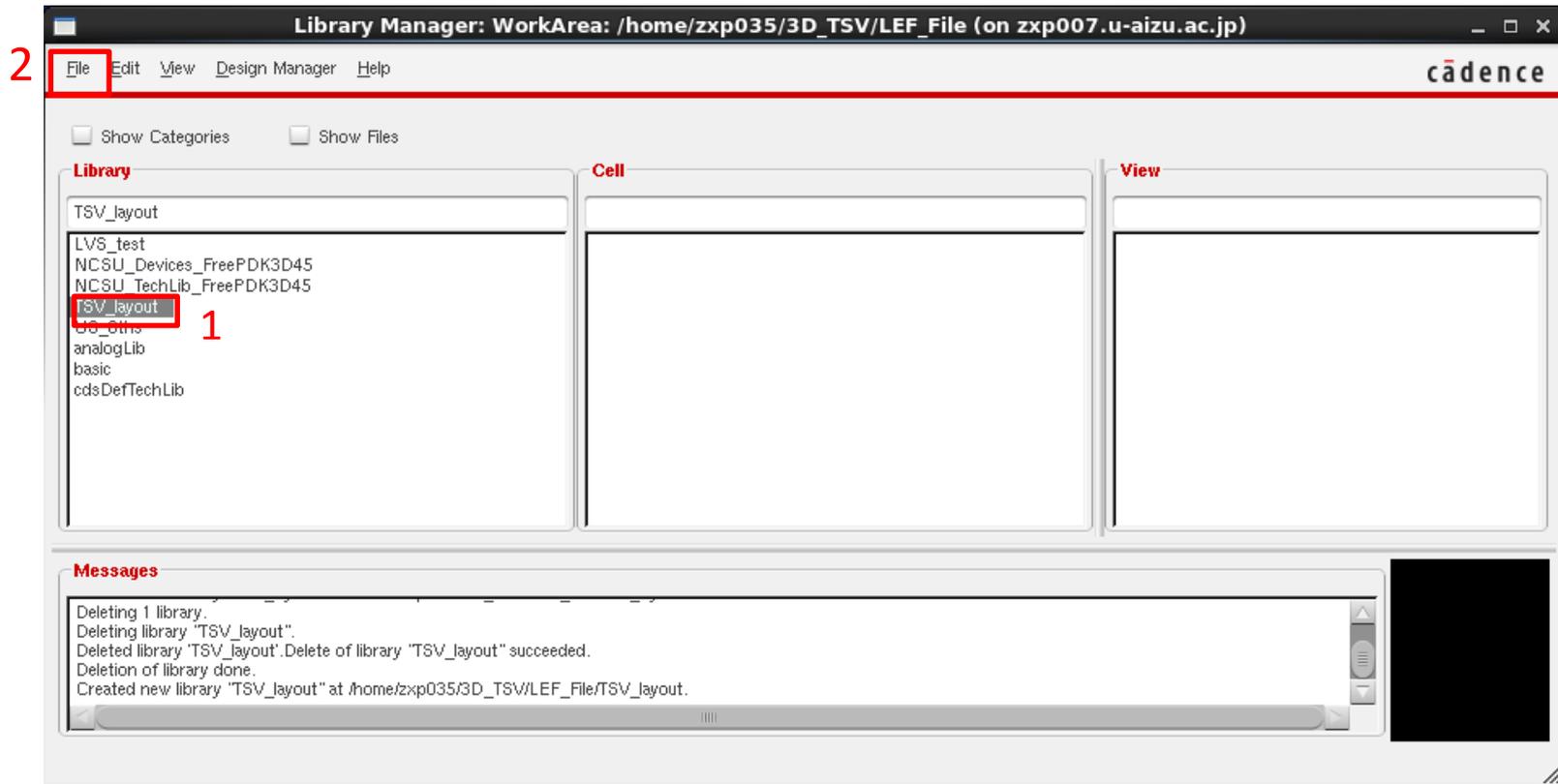
# Step1: Create library b- Technology file



1. Click **NCSU\_TechLib\_FreeFDK3D45**
2. Click -->
3. Click **OK**



# Step2: Create cell view



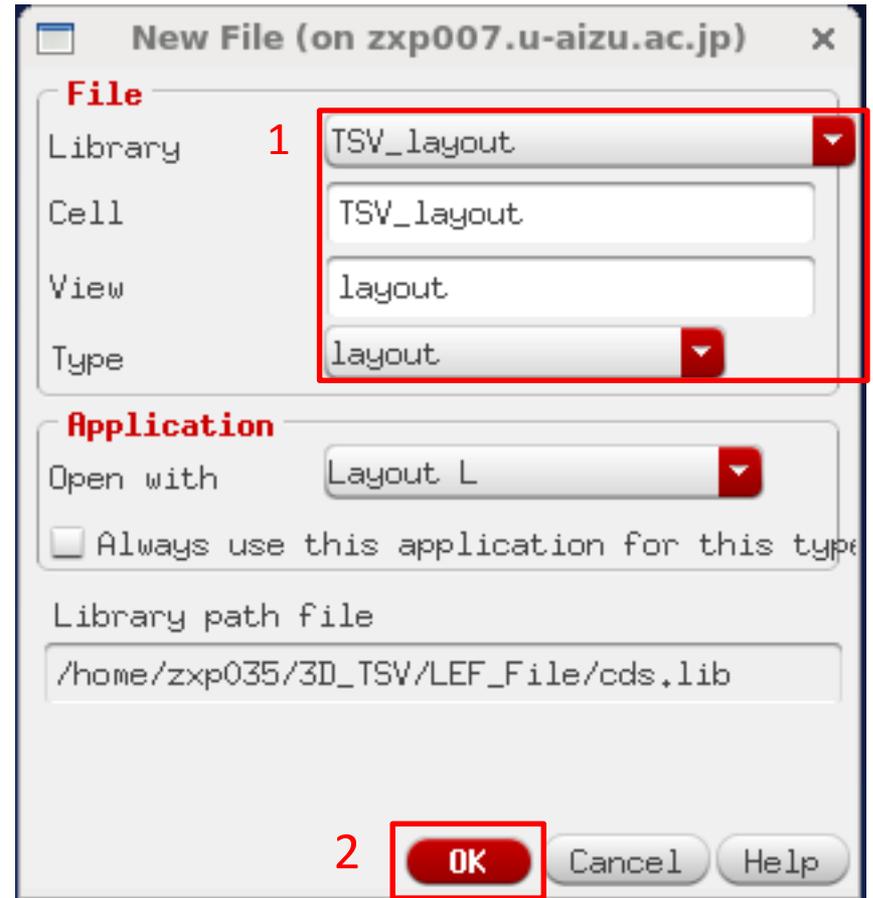
1. Click **TSV\_layout**
2. Click **File -> New -> Cell View** to create cell view



# Step2: Create cell view

1. In File:
  - *Library*: select **TSV\_layout**
  - *Cell*: type **TSV\_layout**
  - *View*: type **layout**
  - *Type*: check **layout**

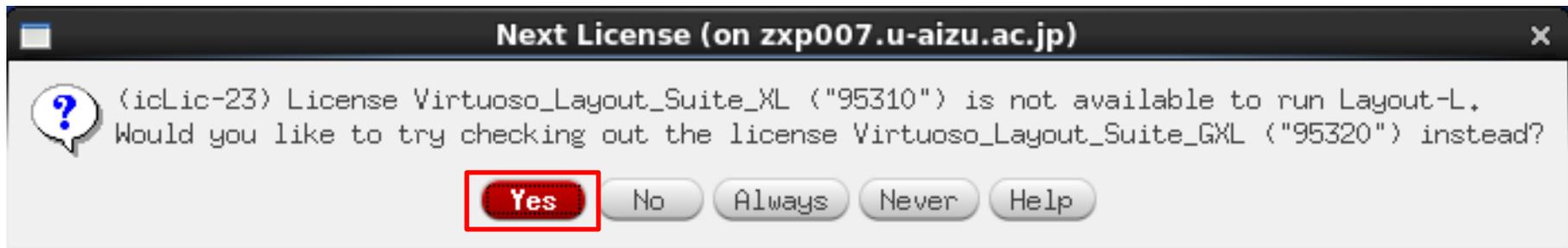
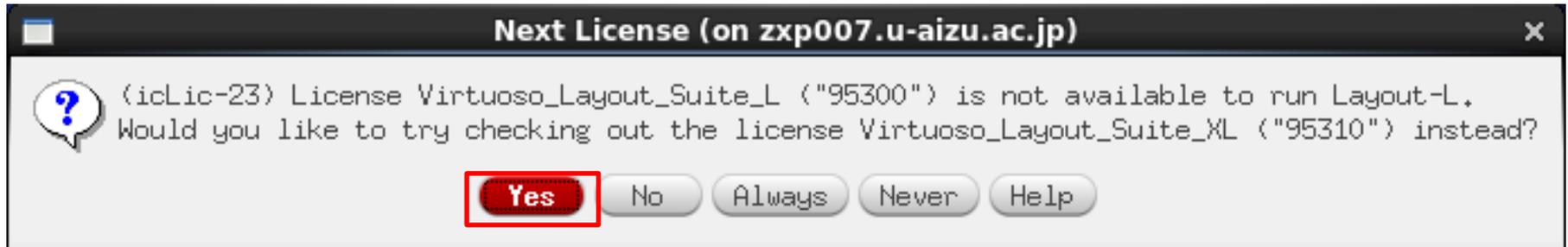
2. Click **OK**





# Step2: Create cell view

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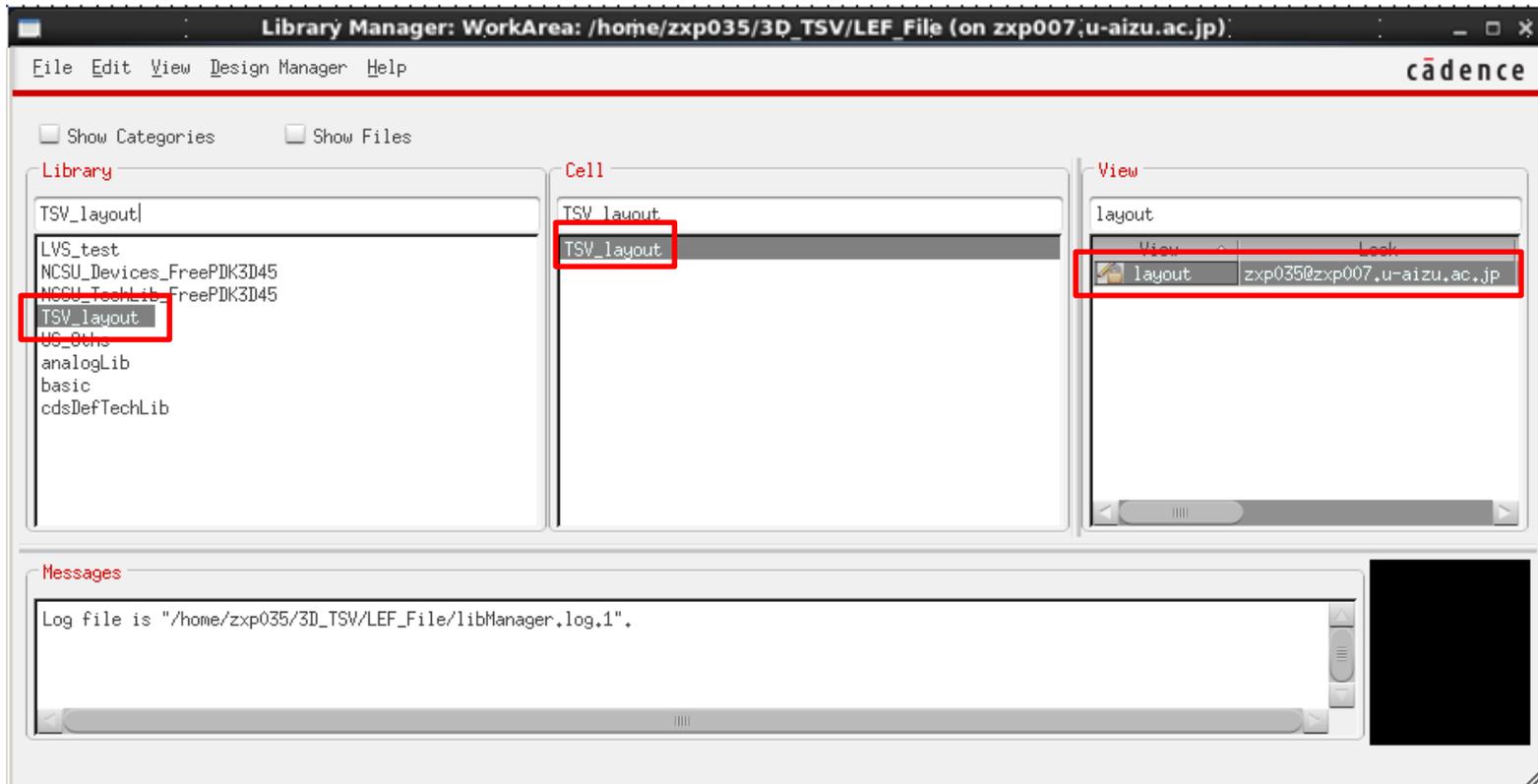


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In both appeared pop-up messages, click **Yes**



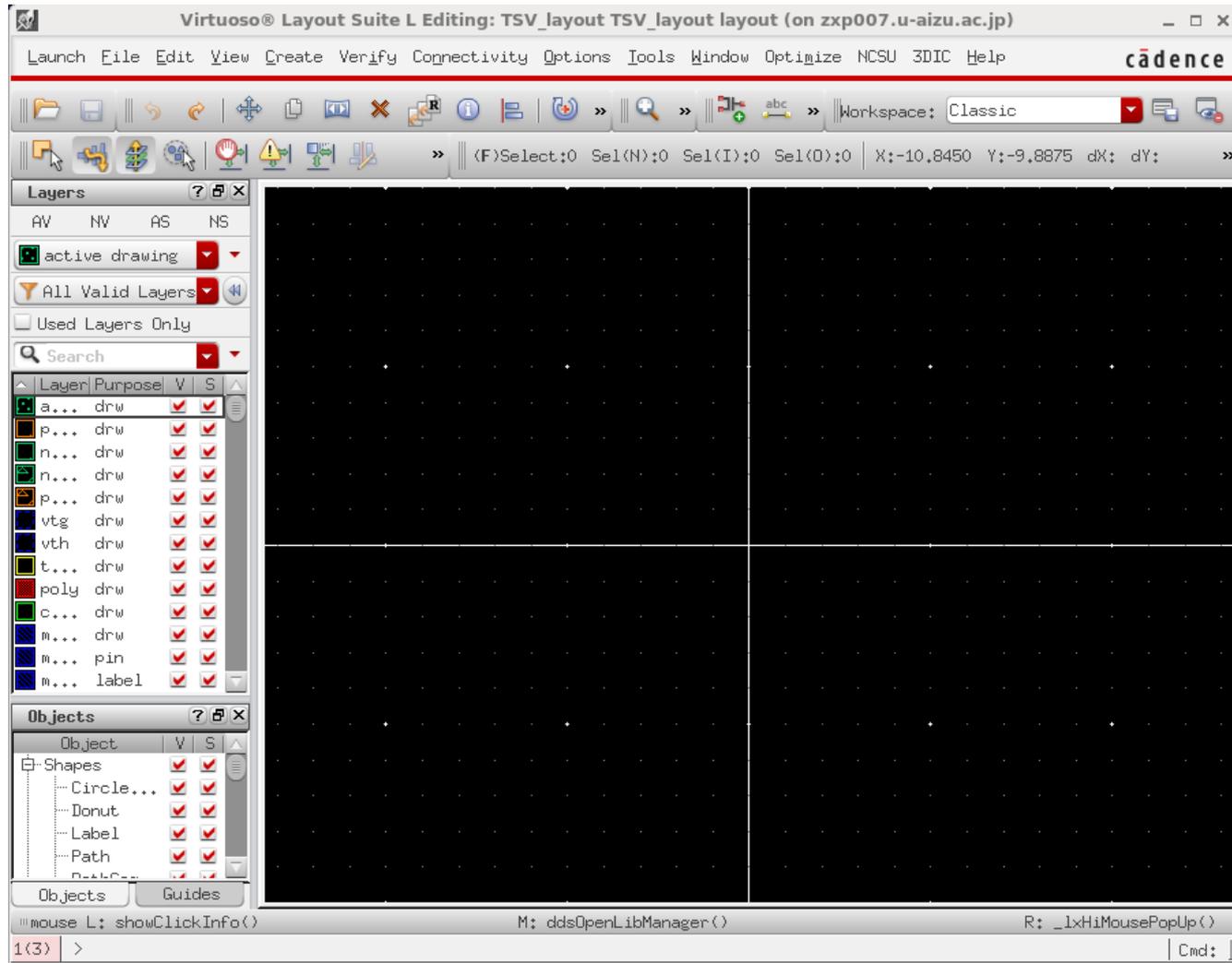
# Step2: Create cell view



Click your library -> Cell -> layout



# Step3: Create TSV layout

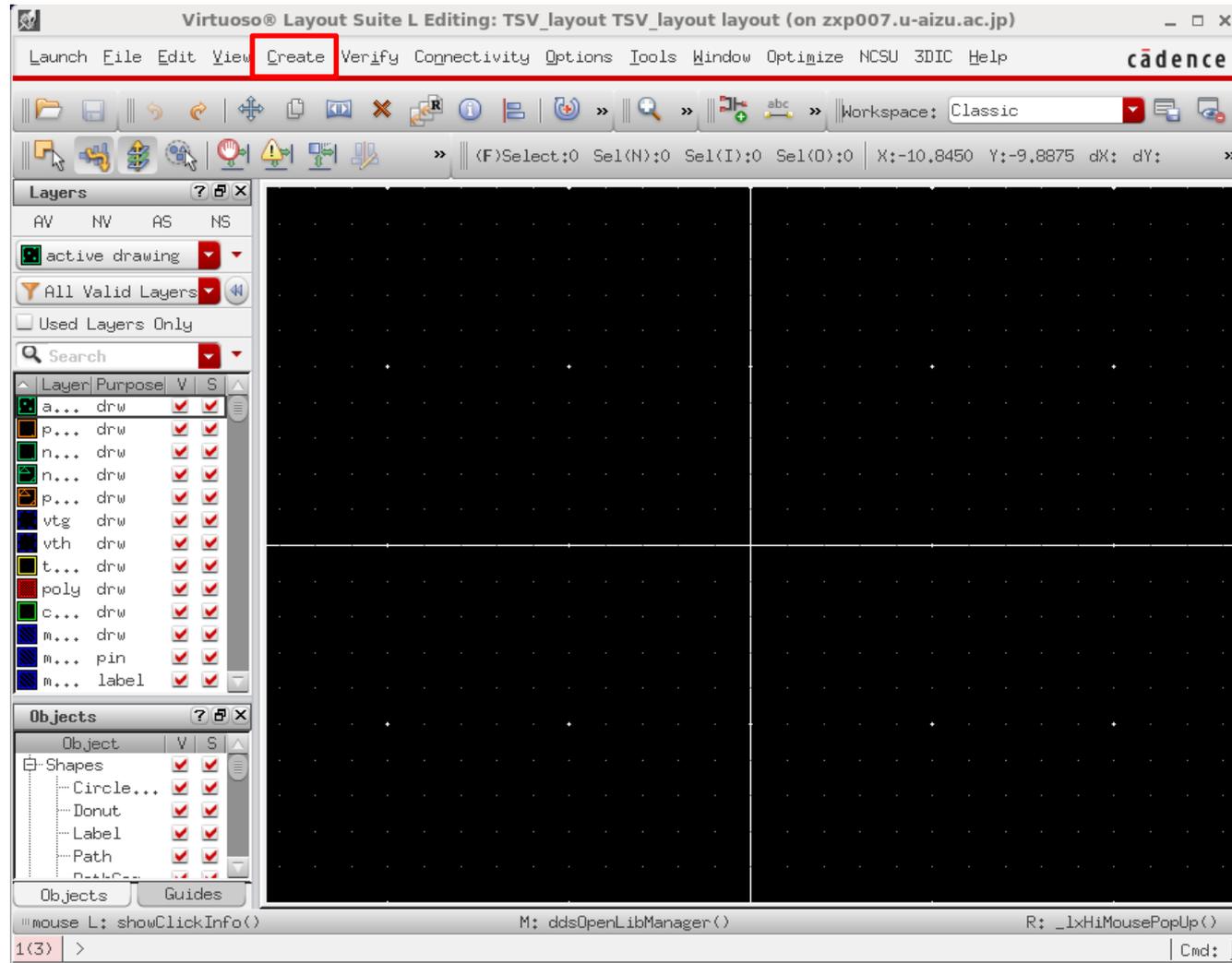


Welcome Virtuoso Layout screen



# Step3: Create TSV layout

## a- Create TSV instance

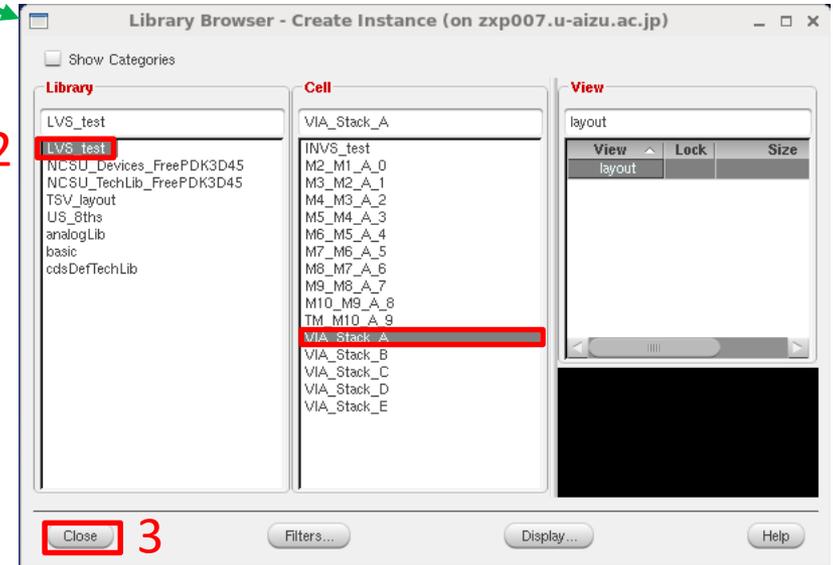
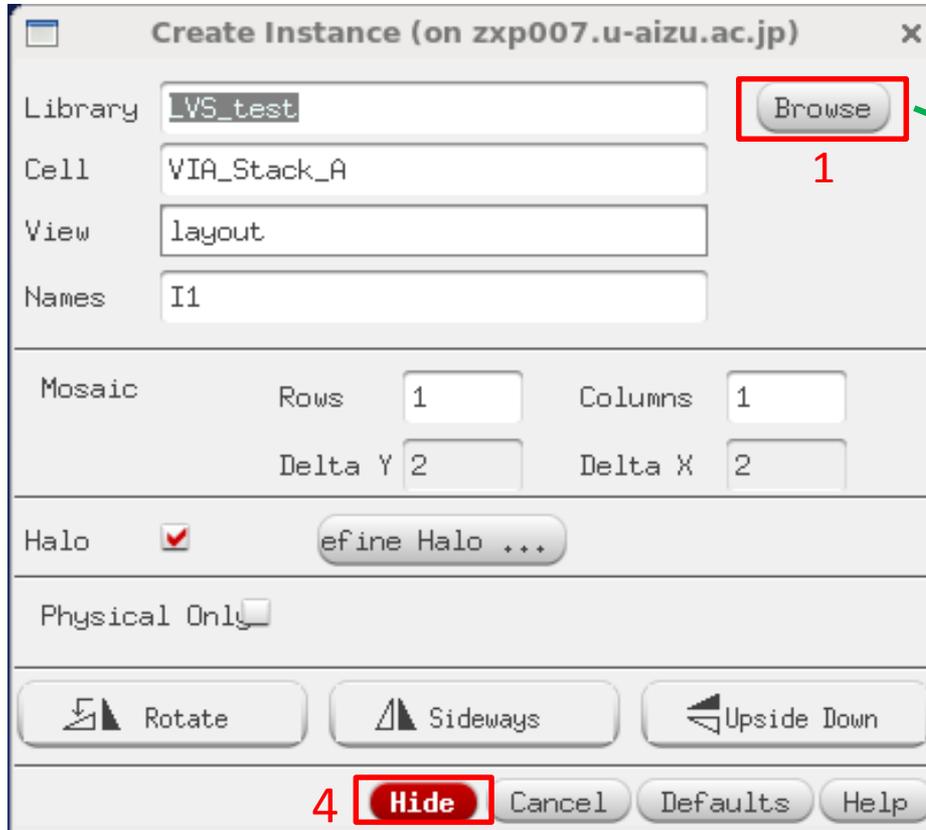


Click Create -> Instance



# Step3: Create TSV layout

## a- Create TSV instance

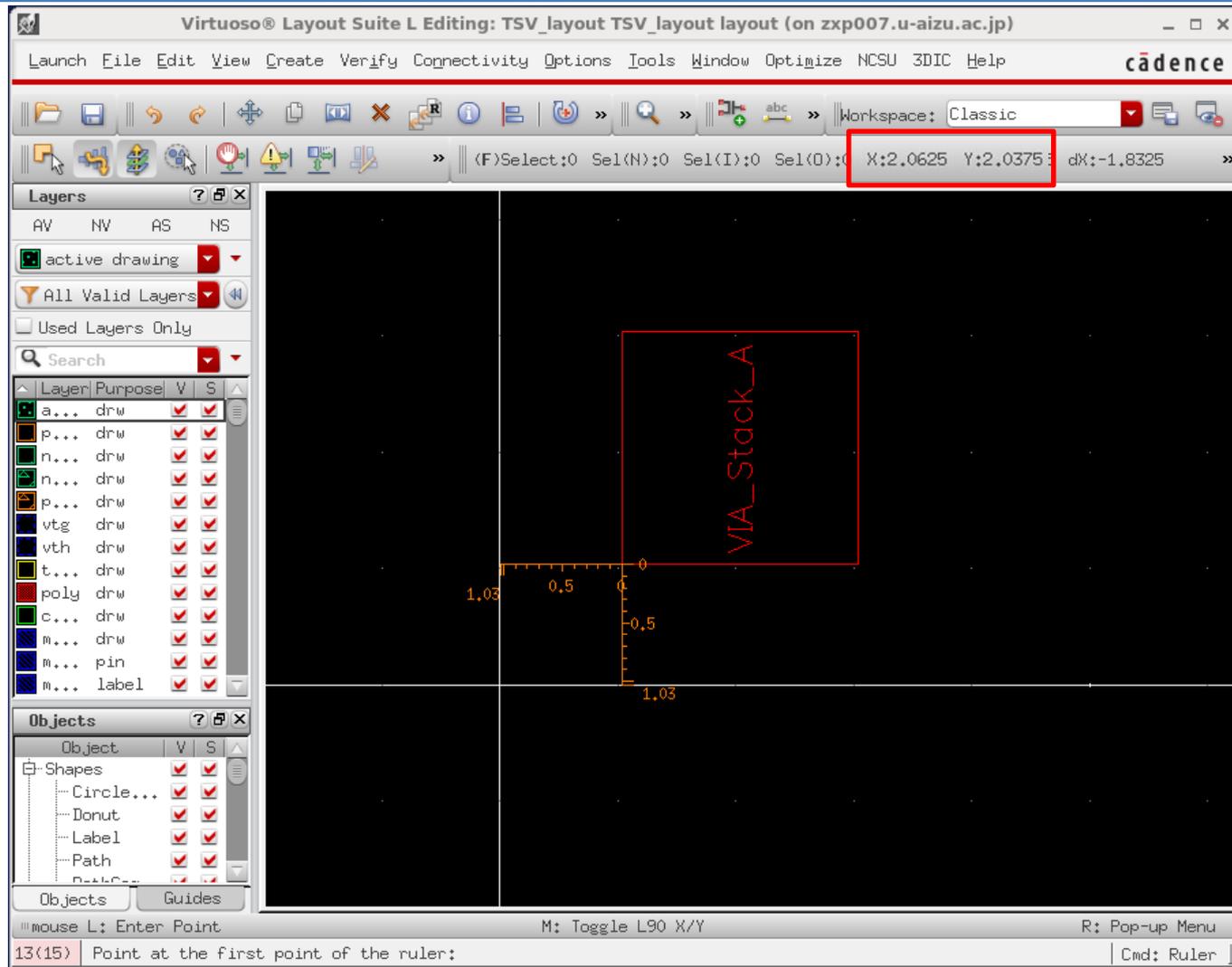


1. Click **Browse**
2. Click **LVS\_test** -> **VIA\_Stack\_A**
3. Click **Close**
4. Click **Hide**



# Step3: Create TSV layout

## a- Create TSV instance



Click **point(X: 2.0625 Y: 2.0375)**.  
You may use the ruler in the toolbar for precision



# Step3: Create TSV layout

## a- Create TSV instance

Edit Instance Properties (on zxp007.u-aizu.ac.jp)

OK Cancel Apply Next Previous Help

Attribute Connectivity Parameter Property ROD DFM Common

Library: LVS\_test

Cell: VIA\_Stack\_A

View: layout

Origin: X: 2.03 (1) Y: 2.03 (2)

Name: I1 Rotation: R0

CellType: none Placement Status: none

Cluster: None Halo...

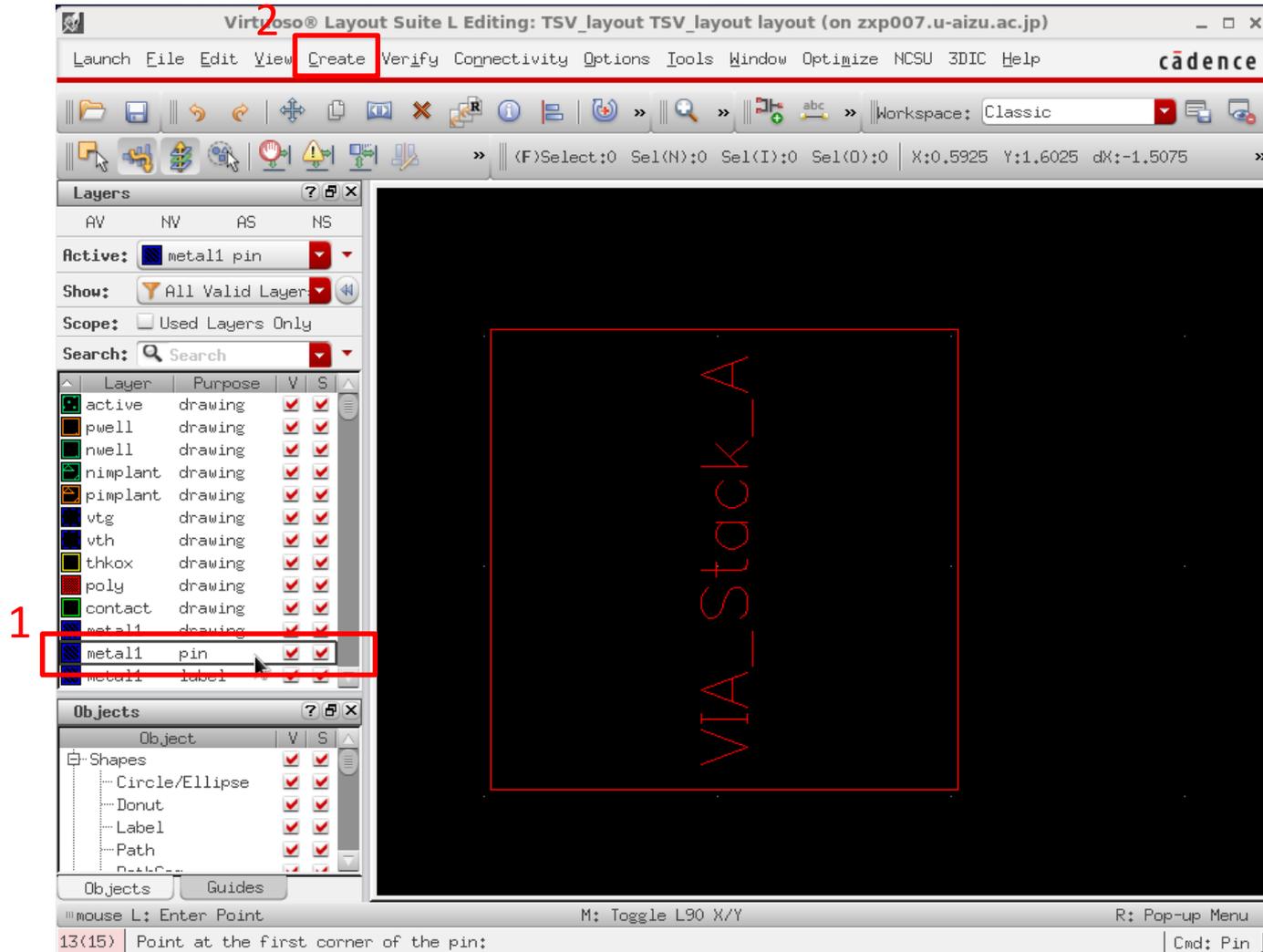
1. In *Origin: X* type **2.03**
2. In *Origin: Y* type **2.03**

Right click on the created **VIA\_Stack\_A**, and click **Properties**



# Step3: Create TSV layout

## b- Create input pin



1. Click **metal1 pin**
2. Click **Create -> Pin**



# Step3: Create TSV layout

## b- Create input pin

1. Terminal Names → **IN**
2. Mode → **rectangle**
3. I/O Type → **input**
4. Click **Hide**

The screenshot shows the 'Create Shape Pin' dialog box with the following settings:

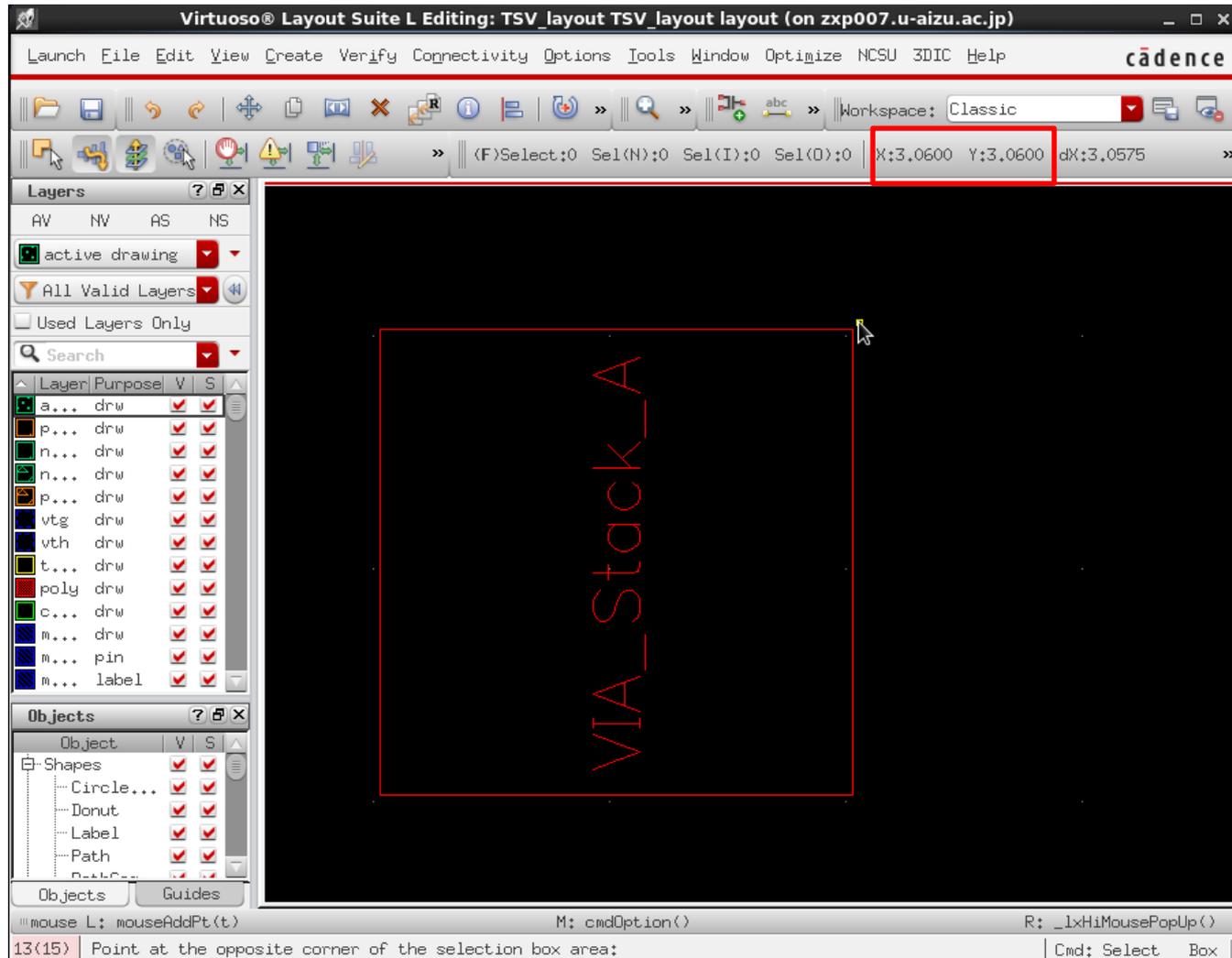
- Connectivity:  strong  weak
- Terminal Names:  Physical Only
- Keep First Name:  X Pitch:  Y Pitch:
- Display Terminal Name:
- Create as ROD Object:
- Name:
- Mode:  rectangle  dot  polygon  circle  auto pin
- I/O Type:  input  output  inputOutput  switch  jumper  unused  tristate
- Snap Mode:
- Access Direction:  Top  Bottom  Left  Right  Any  None
- Buttons:

Red boxes and numbers 1, 2, 3, and 4 highlight the 'Terminal Names' field, the 'rectangle' mode radio button, the 'input' I/O type radio button, and the 'Hide' button, respectively.



# Step3: Create TSV layout

## b- Create input pin

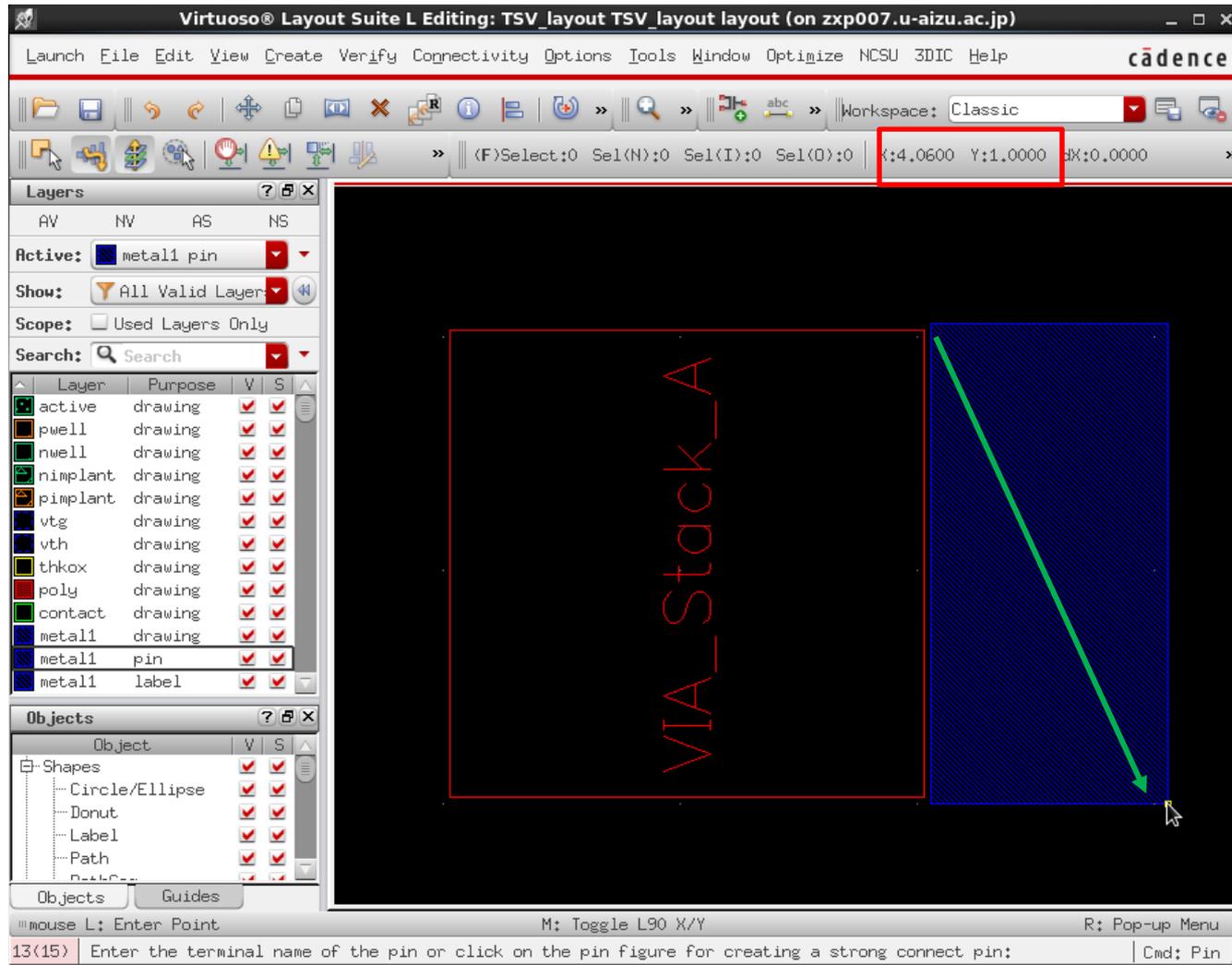


Click point(X:3.06 Y: 3.06)



# Step3: Create TSV layout

## b- Create input pin



Drag the pointer to point(X:4.06 Y: 1.00) and click



# Step3: Create TSV layout

## b- Create input pin

1. Select **metal1 pn**
2. Type  
**Left: 3.06**  
**Right: 4.06**  
**Bottom: 1**  
**Top: 3.06**
3. Click **OK**

3

**Edit Rectangle Pin Properties**

OK Cancel Apply Next Previous

Attribute Connectivity Parameter Property ROD DFM

Layer 1 **metal1 pn** Layer Filter

2

Left	3.06	Bottom	1
Right	4.06	Top	3.06
Width	1	Height	2.06

Placement Status none

Pin Name P\_\_0

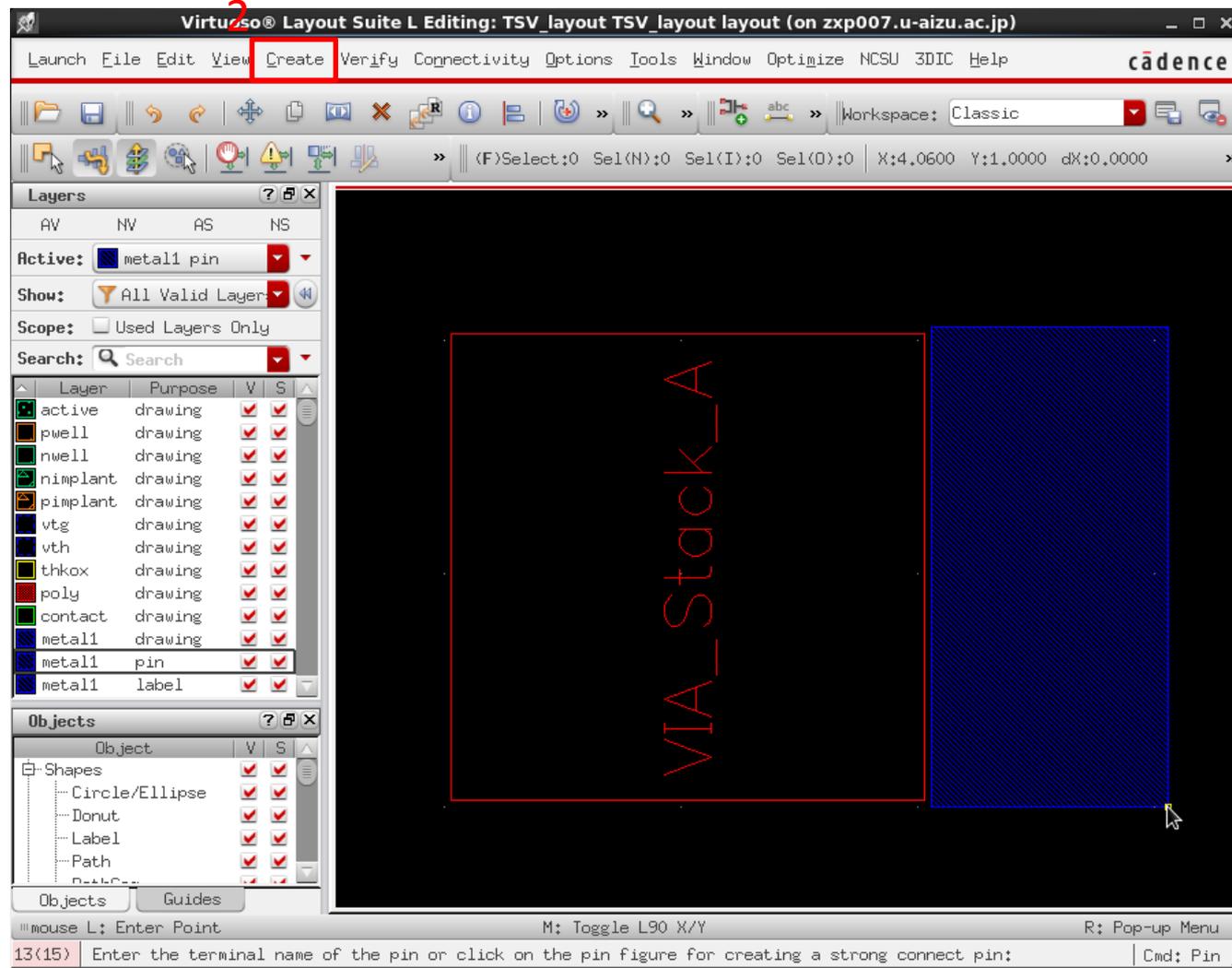
Terminal Name IN

Right click on the created **Input pin** and click **Properties**



# Step3: Create TSV layout

## b- Create input pin



Click Create -> Pin



# Step3: Create TSV layout

## b- Create input pin

1. Type **IN**
2. Check **rectangle**
3. Check **input**
4. Click **Hide**

The screenshot shows the 'Create Shape Pin' dialog box with the following settings and annotations:

- Connectivity:**  strong  weak
- Terminal Names:**  (Annotated with a red box and the number 1)
- Physical Only:**
- Keep First Name:**  X Pitch:  Y Pitch:
- Display Terminal Name:**  (Annotated with a tooltip that says 'Display Terminal Name Option.')
- Create as ROD Object:**
- Name:**
- Mode:**  rectangle  dot  polygon  circle  auto pin (Annotated with a red box and the number 2)
- I/O Type:**  input  output  inputOutput  switch  jumper  unused  tristate (Annotated with a red box and the number 3)
- Snap Mode:**  (Annotated with a red dropdown arrow)
- Access Direction:**  Top  Bottom  Left  Right  Any  None
- Buttons:**  (Annotated with a red box and the number 4), ,



# Step3: Create TSV layout

## b- Create input pin

Virtuoso® Layout Suite L Editing: TSV\_layout TSV\_layout layout (on xzp007.u-aizu.ac.jp)

Launch File Edit View Create Verify Connectivity Options Tools Window Optimize NCSU 3DIC Help cadence

Workspace: Classic

X:4.0600 Y:1.0000 dX:0.8125

Layers

AV NV AS NS

Active: metal1 pin

Show: All Valid Layer

Scope: Used Layers Only

Search: Search

Layer	Purpose	V	S
active	drawing	✓	✓
pwell	drawing	✓	✓
nwell	drawing	✓	✓
nimplant	drawing	✓	✓
pimplant	drawing	✓	✓
vtg	drawing	✓	✓
vth	drawing	✓	✓
thkox	drawing	✓	✓
poly	drawing	✓	✓
contact	drawing	✓	✓
metal1	drawing	✓	✓
metal1	pin	✓	✓
metal1	label	✓	✓

Objects

Object	V	S
Shapes	✓	✓
Circle/Ellipse	✓	✓
Donut	✓	✓
Label	✓	✓
Path	✓	✓

mouse L: Enter Point M: Toggle L90 X/Y R: Pop-up Menu

13(15) Point at the first corner of the pin: Cmd: Pin

Click point(X:4.06 Y: 1.00)



# Step3: Create TSV layout

## b- Create input pin

Virtuoso® Layout Suite L Editing: TSV\_layout TSV\_layout layout (on zxp007.u-aizu.ac.jp)

Launch File Edit View Create Verify Connectivity Options Tools Window Optimize NCSU 3DIC Help cadence

Workspace: Classic

X:0.0000 Y:0.0000 dX:-4.0600

Layers

AV NV AS NS

Active: metal1 pin

Show: All Valid Layers

Scope: Used Layers Only

Search: Search

Layer	Purpose	V	S
active	drawing	✓	✓
pwell	drawing	✓	✓
nwell	drawing	✓	✓
nimplant	drawing	✓	✓
pimplant	drawing	✓	✓
vtg	drawing	✓	✓
vth	drawing	✓	✓
thkox	drawing	✓	✓
poly	drawing	✓	✓
contact	drawing	✓	✓
metal1	drawing	✓	✓
metal1	pin	✓	✓
metal1	label	✓	✓

Objects

Object	V	S
Shapes	✓	✓
Circle/Ellipse	✓	✓
Donut	✓	✓
Label	✓	✓
Path	✓	✓
PathCap	✓	✓

mouse L: Enter Point M: Toggle L90 X/Y R: Pop-up Menu

13(15) Point at the opposite corner of the pin; Cmd: Pin

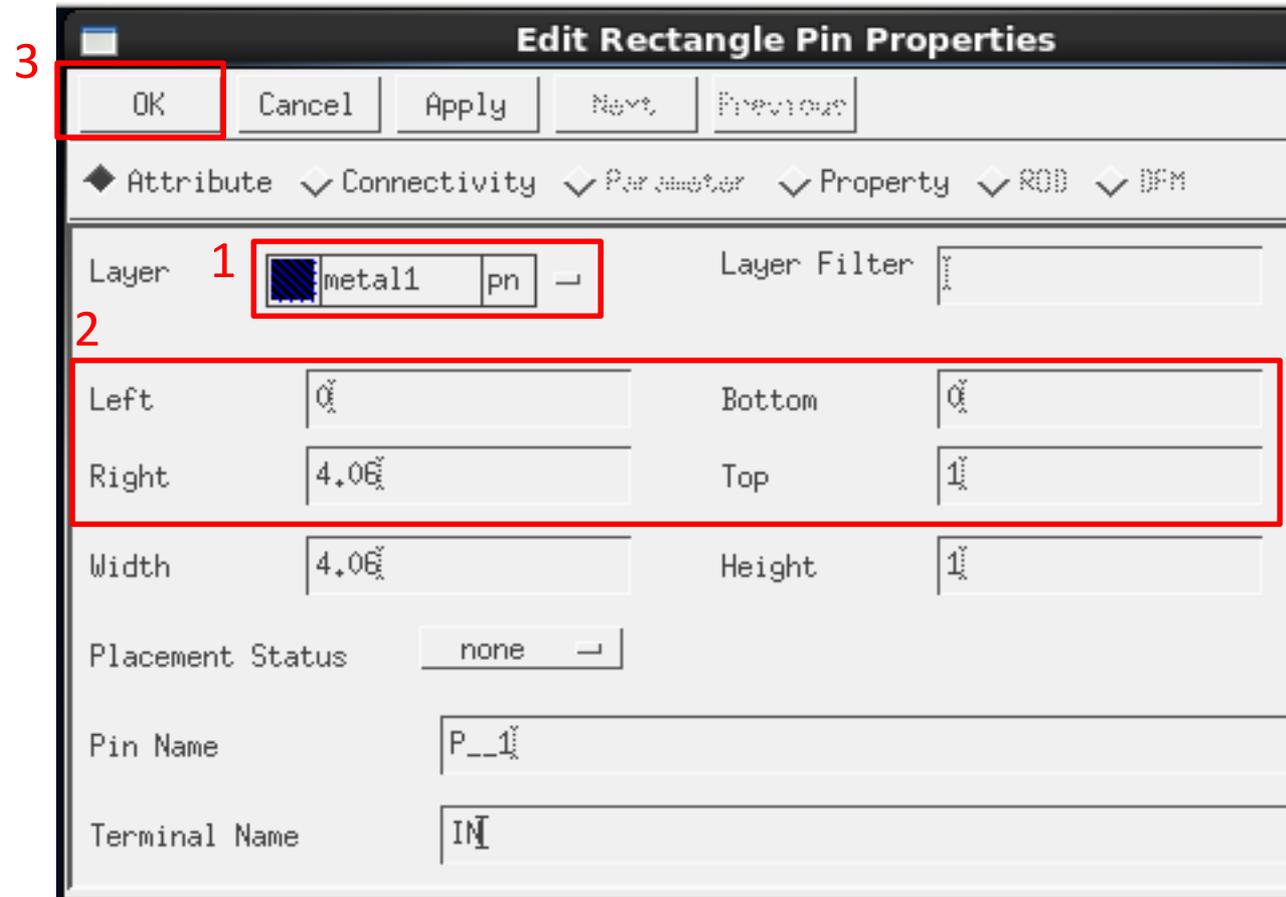
Drag the pointer to point(X:0.00 Y: 0.00) and click



# Step3: Create TSV layout

## b- Create input pin

1. Select **metal1 pn**
2. Type  
**Left: 0**  
**Right: 4.06**  
**Bottom: 0**  
**Top: 1**
3. Click **OK**



Right click created **Input pin** and click **Properties**



# Step3: Create TSV layout

## b- Create input pin

Virtuoso® Layout Suite L Editing: TSV\_layout TSV\_layout layout (on zxp007.u-aizu.ac.jp)

Launch File Edit View Create Verify Connectivity Options Tools Window Optimize NCSU 3DIC Help cadence

Workspace: Classic

(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:-0.1150 Y:3.3325 dX:-4.1750

Layers

AV NV AS NS

Active: metal1 pin

Show: All Valid Layers

Scope: Used Layers Only

Search: Search

Layer	Purpose	V	S
active	drawing	✓	✓
pwell	drawing	✓	✓
nwell	drawing	✓	✓
nimplant	drawing	✓	✓
pimplant	drawing	✓	✓
vtg	drawing	✓	✓
vth	drawing	✓	✓
thkox	drawing	✓	✓
poly	drawing	✓	✓
contact	drawing	✓	✓
metal1	drawing	✓	✓
metal1 pin		✓	✓
metal1 label		✓	✓

Objects

Object	V	S
Shapes	✓	✓
Circle/Ellipse	✓	✓
Donut	✓	✓
Label	✓	✓
Path	✓	✓

Objects Guides

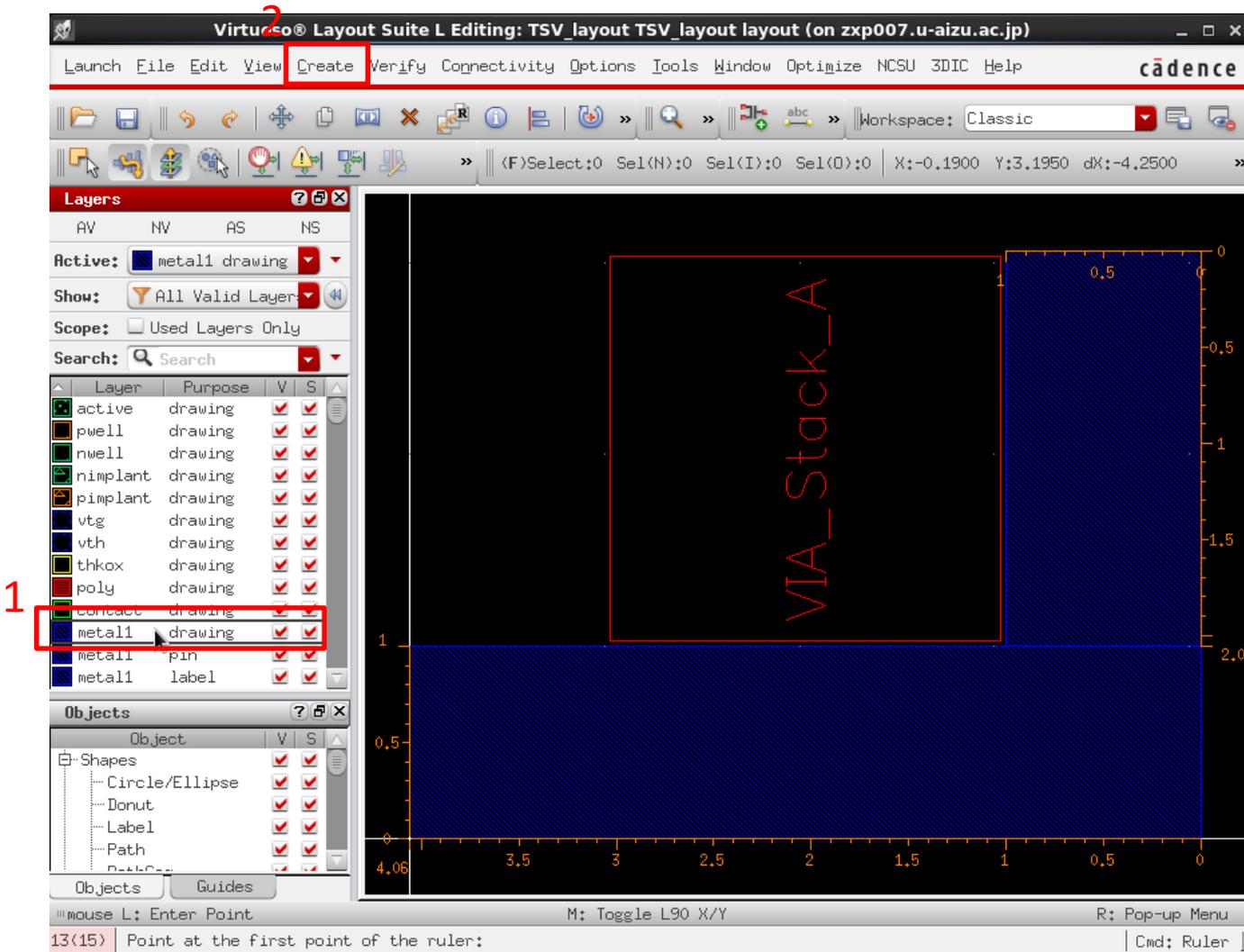
mouse L: Enter Point M: Toggle L90 X/Y R: Pop-up Menu

13(15) Point at the first point of the ruler: Cmd: Ruler



# Step3: Create TSV layout

## c- Create path

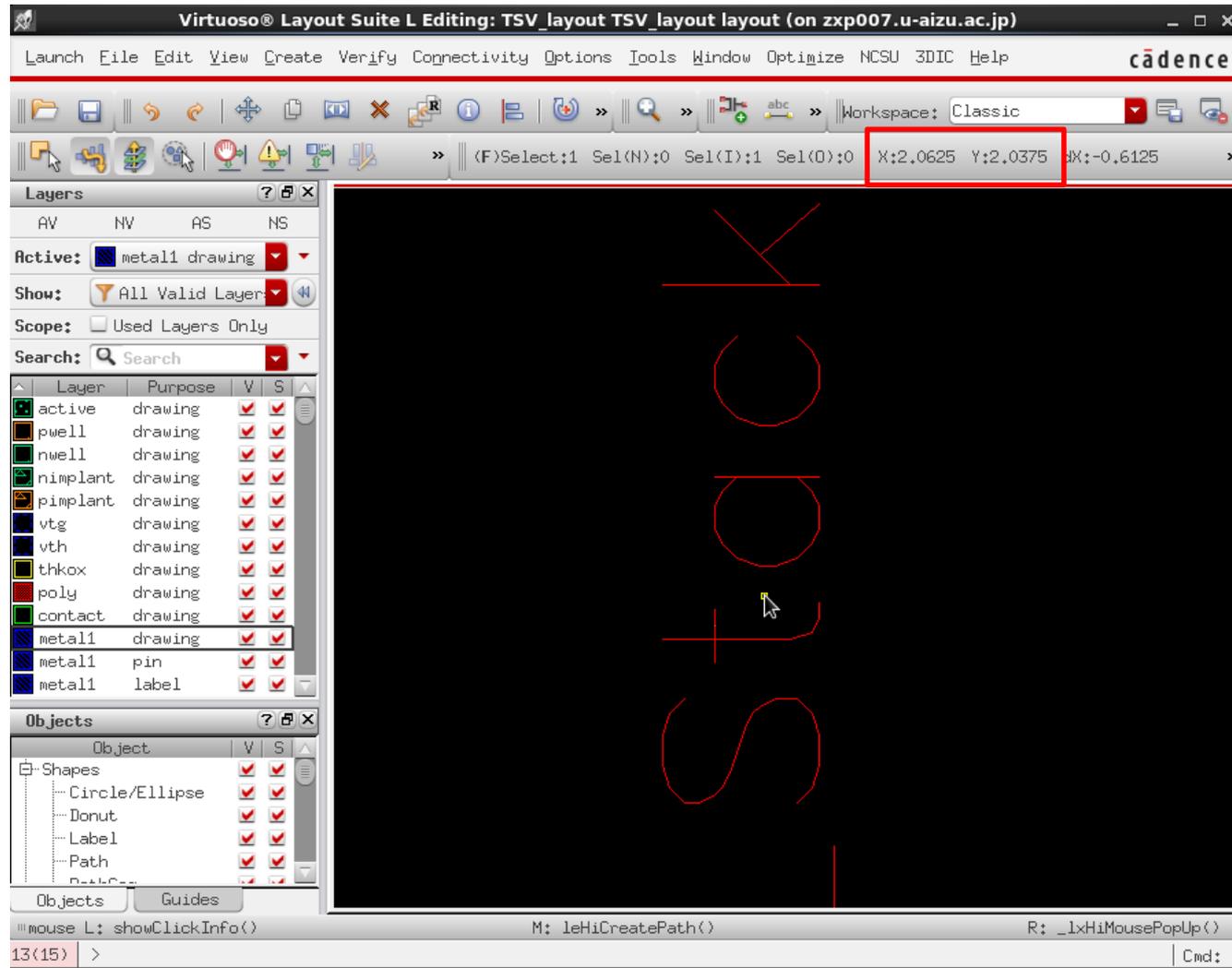


1. Click metal1 drawing
2. Click Create -> Shape -> path



# Step3: Create TSV layout

## c- Create path

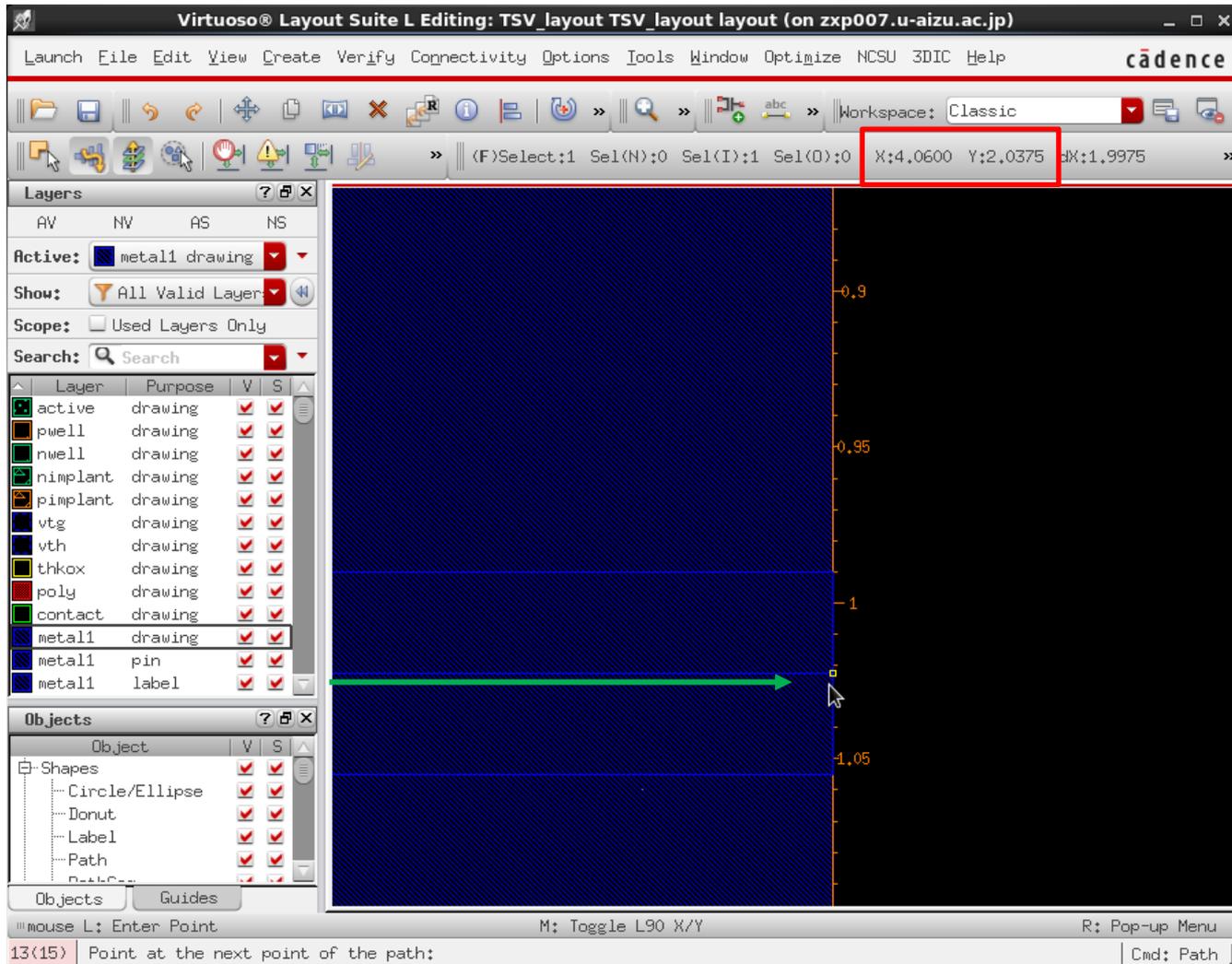


Click point(X: 2.0625 Y: 2.0375)



# Step3: Create TSV layout

## c- Create path

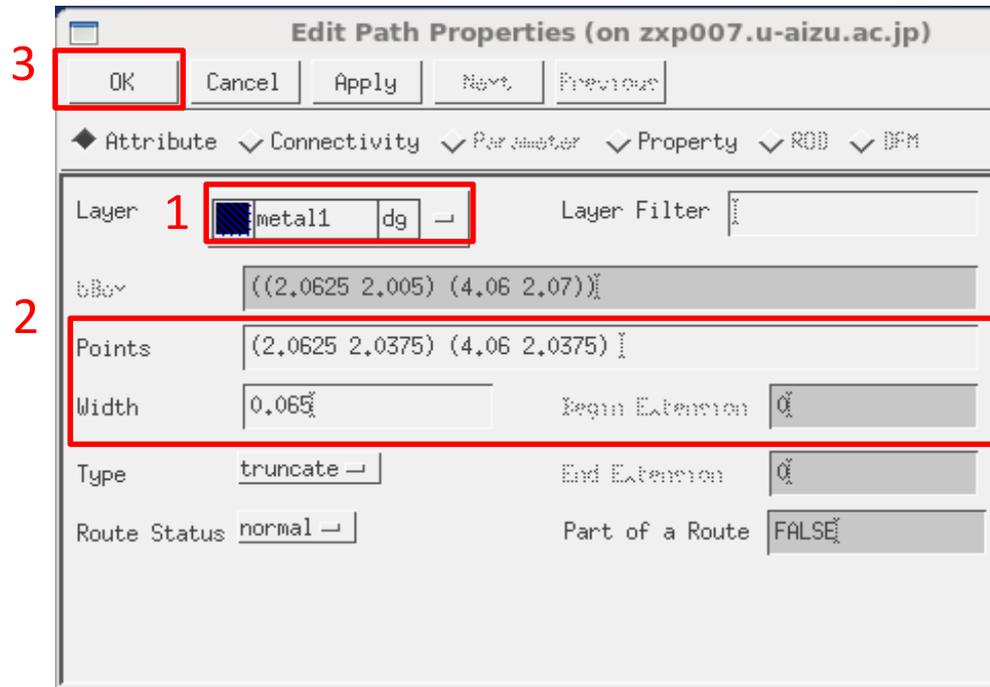


Drag the pointer to point(X:4.06 Y: 2.0375) and double click



# Step3: Create TSV layout

## c- Create path



1. Select **metal1 dg**
2. Type  
Points: **(2.0625 2.0375) (4.06 2.0375)**  
Width: **0.065**
3. Click **OK**

Right click on the created **path** and click **Properties**



# Step3: Create TSV layout d- Create output pin

Virtuoso® Layout Suite L Editing: TSV\_layout TSV\_layout layout (on zxp007.u-aizu.ac.jp)

Launch File Edit View **Create** Verify Connectivity Options Tools Window Optimize NCSU 3DIC Help

Workspace: Classic

(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:-0.2250 Y:1.8050 dX:-4.2850

**Layers**

AV NV AS NS

Active: TM pin

Show: All Valid Layers

Scope: Used Layers Only

Search: TM

Layer	Purpose	V	S
TM	drawing	✓	✓
TM	pin	✓	✓
TM	label	✓	✓
TM_A	drawing	✓	✓
TM_A	pin	✓	✓
TM_A	label	✓	✓
TM_B	drawing	✓	✓
TM_B	pin	✓	✓
TM_B	label	✓	✓
TM_C	drawing	✓	✓
TM_C	pin	✓	✓
TM_C	label	✓	✓
TM_D	drawing	✓	✓

**Objects**

Object	V	S
Shapes	✓	✓
Circle/Ellipse	✓	✓
Donut	✓	✓
Label	✓	✓
Path	✓	✓

mouse L: Enter Point M: Toggle L90 X/Y R: Pop-up Menu

13(15) Point at the first corner of the pin: Cmd: Pin

1. Click **TM pin**
2. Click **Create -> pin**



# Step3: Create TSV layout

## d- Create output pin

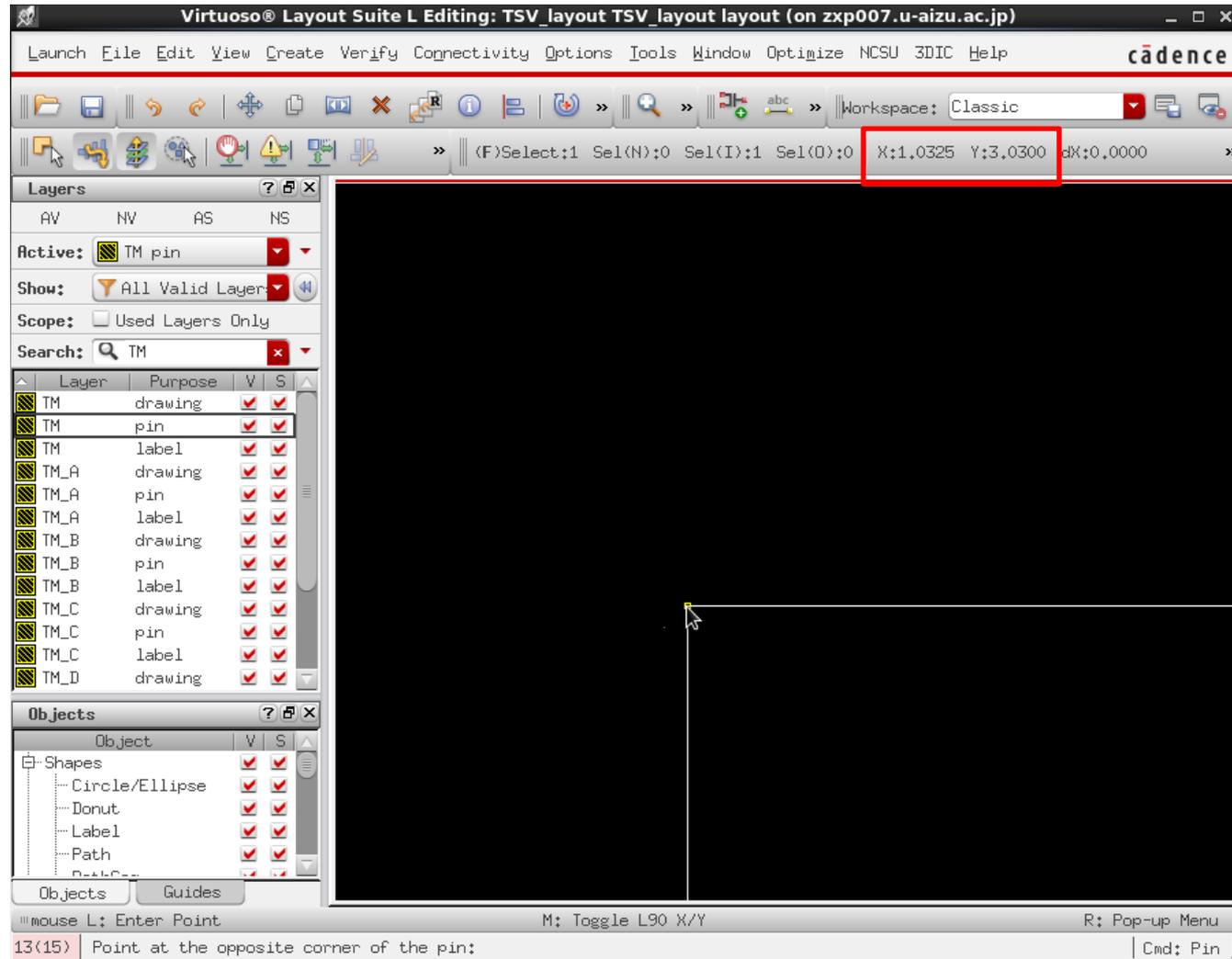
1. Type **OUT**
2. Check **rectangle**
3. Check **output**
4. Click **Hide**

The screenshot shows the 'Create Shape Pin' dialog box for a file named 'zxp007.u-aizu.ac.jp'. The dialog is divided into several sections:

- Connectivity:** 'strong' is selected (indicated by a red circle and the number '1').
- Terminal Names:** The text 'OUT' is entered in the input field (indicated by a red box and the number '1').
- Options:** 'Keep First Name', 'Display Terminal Name', and 'Create as ROD Object' are unchecked. 'Physical Only' is also unchecked.
- Name:** The default name 'rect0' is shown in the input field.
- Mode:** 'rectangle' is selected (indicated by a red box and the number '2').
- I/O Type:** 'output' is selected (indicated by a red box and the number '3').
- Snap Mode:** 'orthogonal' is selected in the dropdown menu.
- Access Direction:** 'Top', 'Bottom', 'Left', and 'Right' are all checked.
- Buttons:** The 'Hide' button is highlighted with a red box and the number '4'. 'Cancel' and 'Help' buttons are also visible.



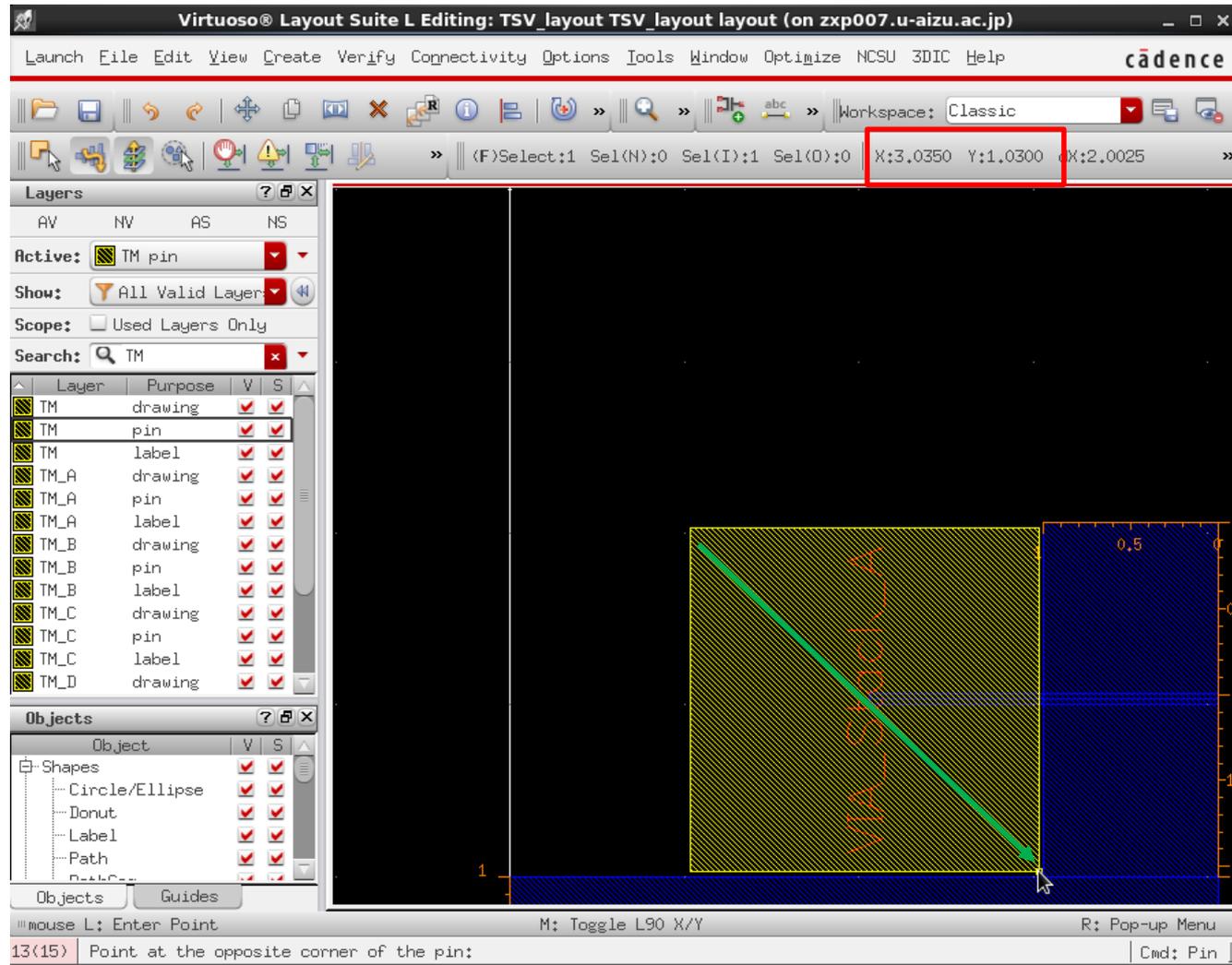
# Step3: Create TSV layout d- Create output pin



Click point(X: 1.03 Y: 3.03)



# Step3: Create TSV layout d- Create output pin



Drag the pointer to point(X:3.03 Y: 1.03) and click



# Step3: Create TSV layout

## d- Create output pin

1. Select **TM pn**
2. Type  
**Left: 1.03**  
**Right: 3.03**  
**Bottom: 1.03**  
**Top: 3.03**
3. Click **OK**

3

OK Cancel Apply Next Previous

◆ Attribute ▾ Connectivity ▾ Parameter ▾ Property ▾ ROD ▾ DFM

Layer 1 **TM pn** Layer Filter

2

Left	1.03	Bottom	1.03
Right	3.03	Top	3.03

Width 2 Height 2

Placement Status none ▾

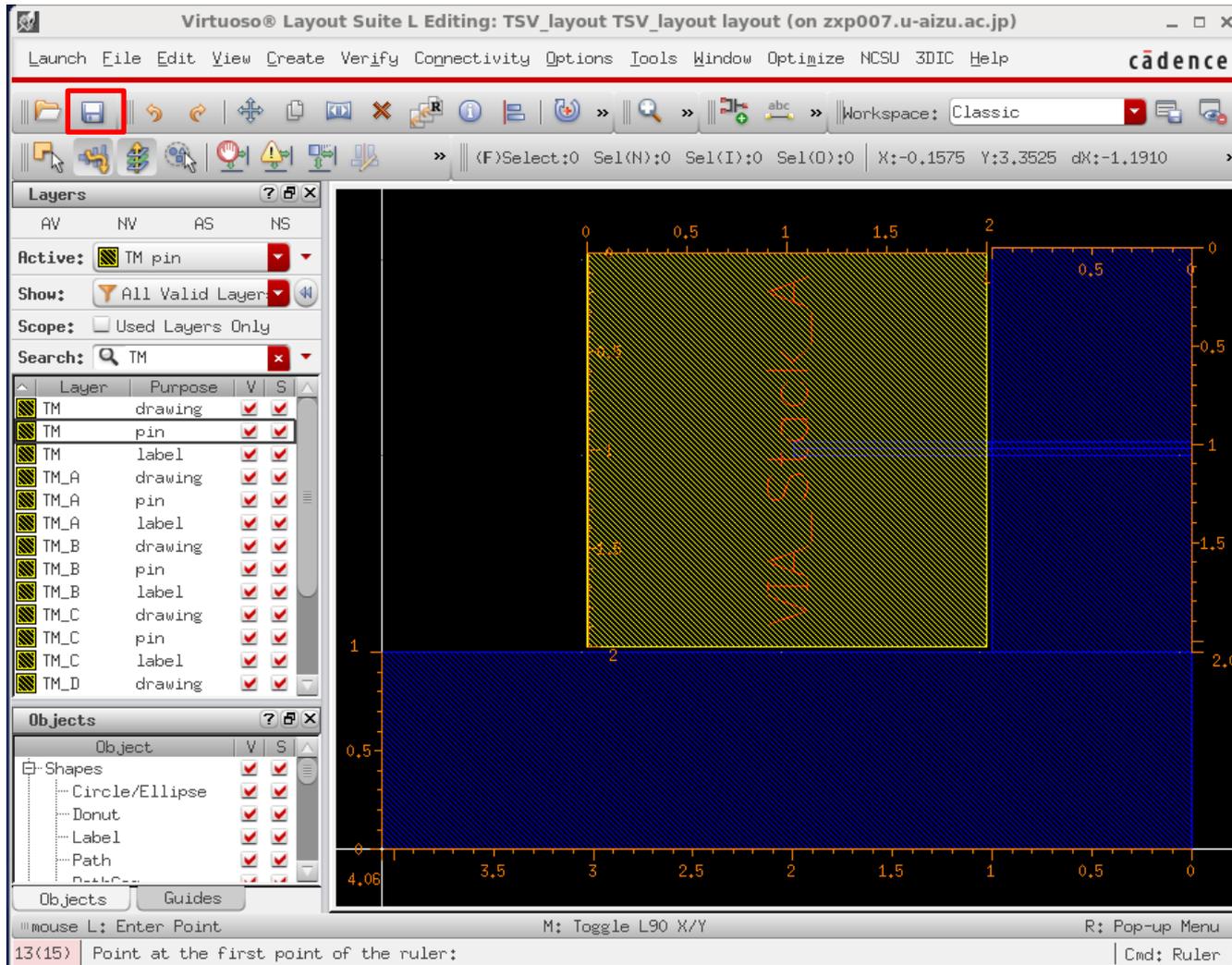
Pin Name P\_2

Terminal Name OUT

Right click **created Output pin** and click **Properties**



# Step3: Create TSV layout

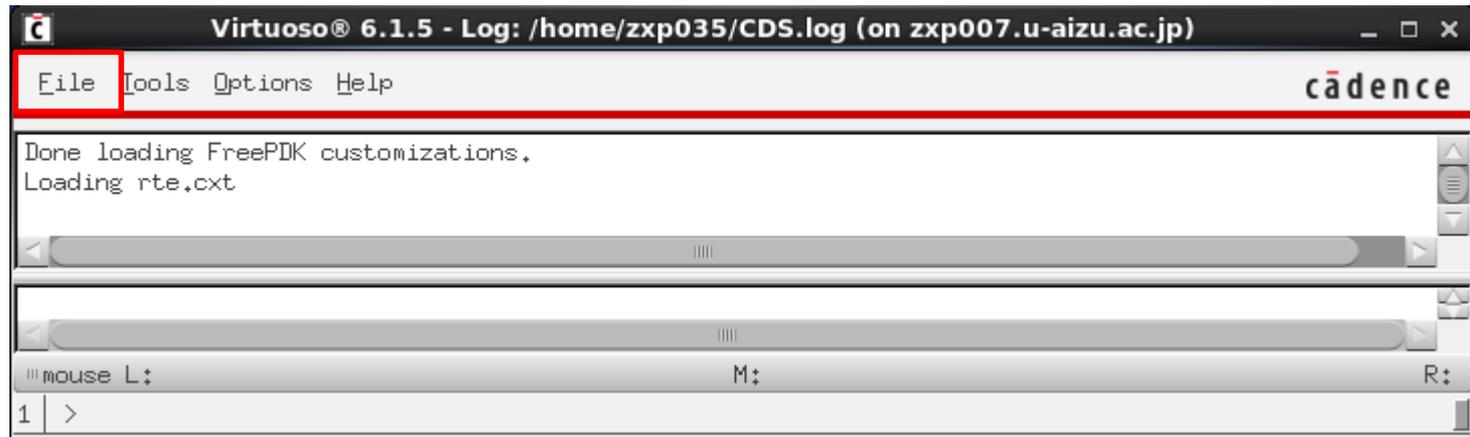


The TSV layout is completed.

Click the **Save Icon**



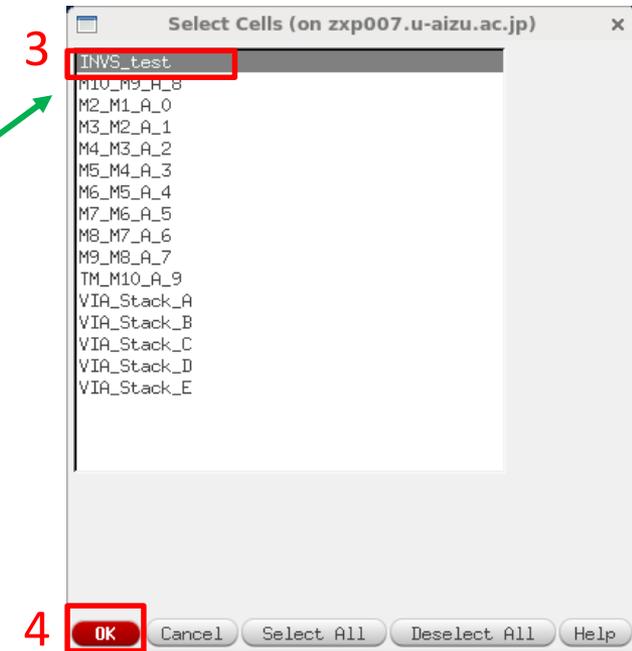
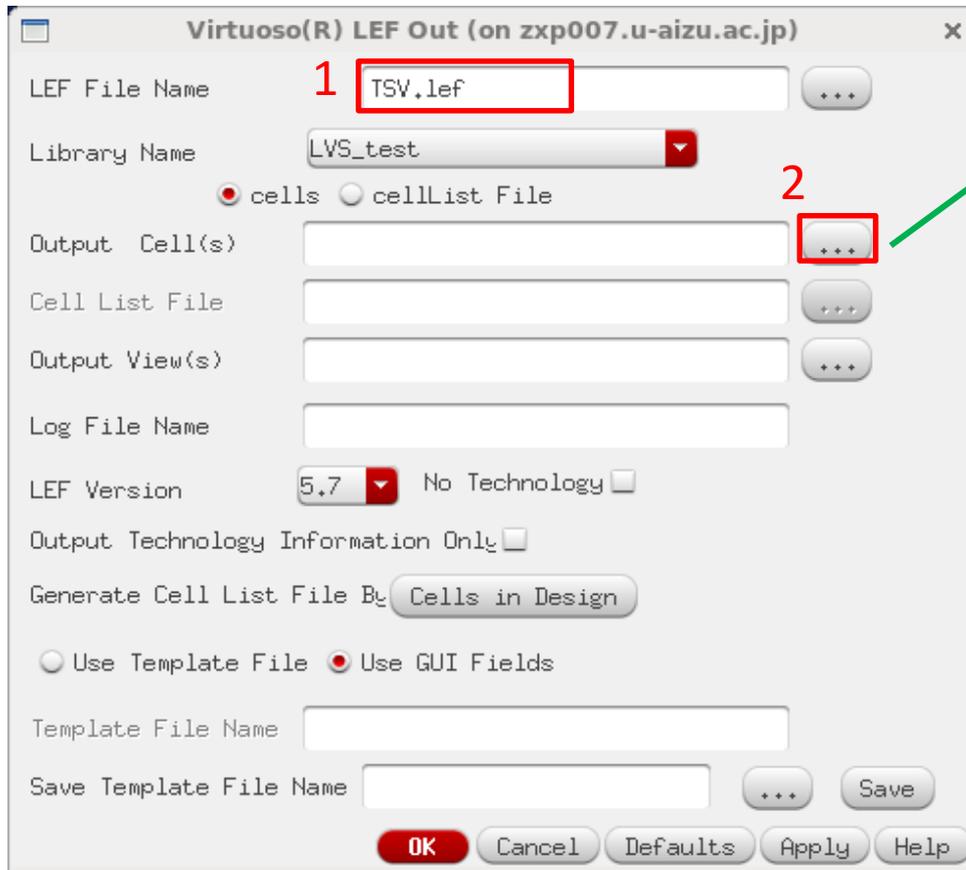
# Step4: Export LEF



Click **File** -> **Export** -> **Lef** to create lef file



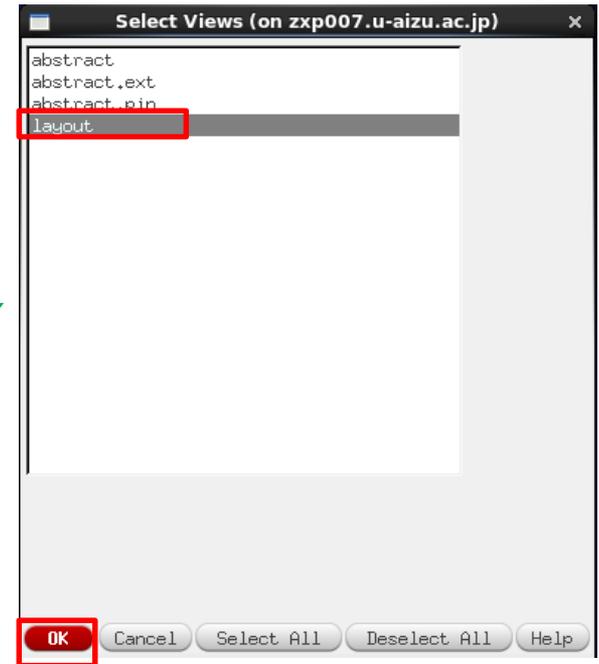
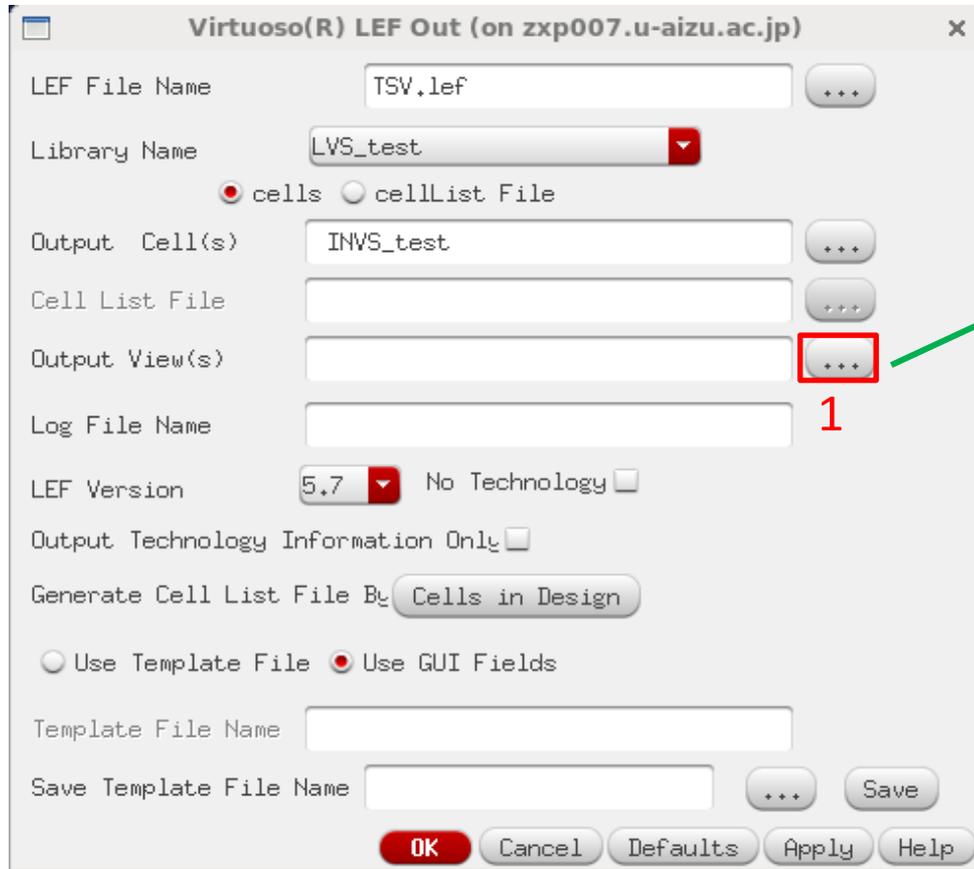
# Step4: Export LEF



1. In *LEF File Name*, Type **TSV.lef**
2. Click on **Output Cell**
3. Click **INVS\_test**
4. Click **OK**



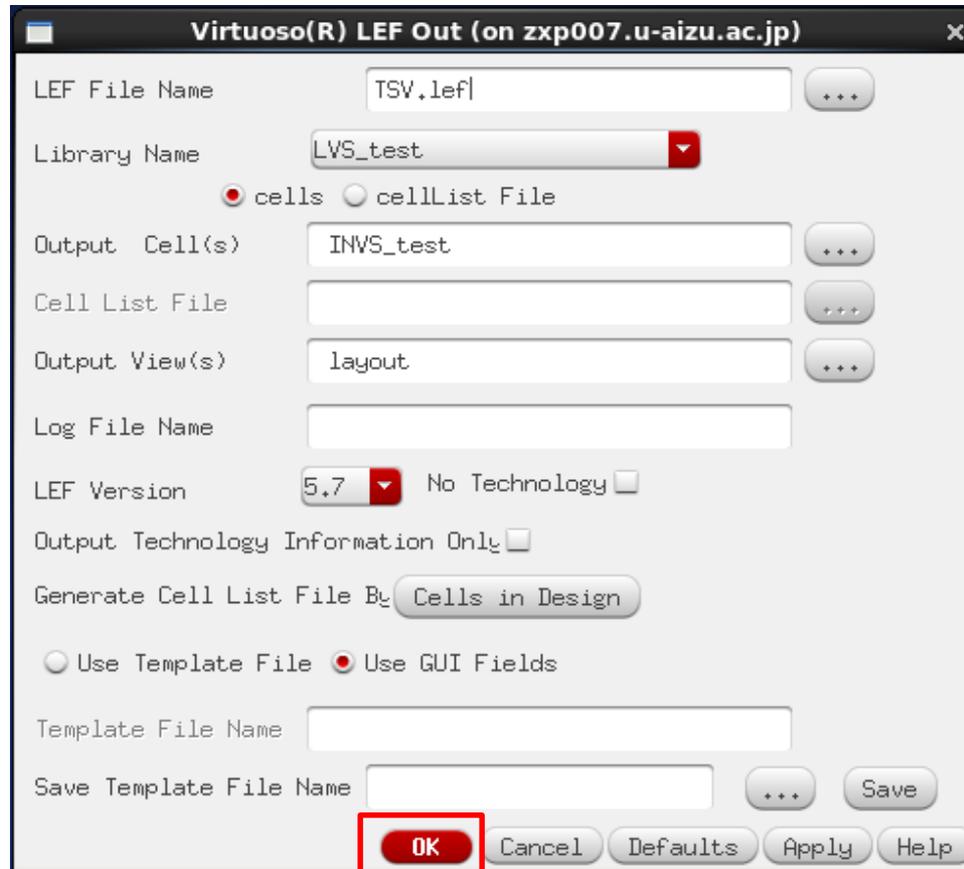
# Step4: Export LEF



1. Click on **Output View**
2. Click **layout**
3. Click **OK**



# Step4: Export LEF



Click **OK**



# Step4: Export LEF

```
Virtuoso® 6.1.5 - Log: /home/zxp035/CDS.log (on zxp007.u-aizu.ac.jp)
File Tools Options Help
cadence

Host Name : zxp007.u-aizu.ac.jp
Directory : /home/zxp035/3D_TSV/LEF_File
DB Version: 20110110 (SJ)
CADENCE Design Systems, Inc.
*****
Running: lefout -lib LVS_test -cells "INVS_test" -views "layout" -lef /home/zxp035/3D_TSV/LEF_File/TSV.lef -
WARNING: (0ALEFDEF-50144): NONDEFAULTRULE virtuosoDefaultExtractorSetup; LAYER via9; invalid definition. The
WARNING: (0ALEFDEF-90016): Design INVS_test layout does not have a snapBoundary. Searching for a prBoundary.
WARNING: (0ALEFDEF-90017): Design INVS_test layout does not have a prBoundary. Searching for a layer-purpose
WARNING: (0ALEFDEF-90018): No shape on layer purpose pair found in the design INVS_test layout. The ORIGIN,

Elapsed Time: 1.9s

lefout translation completed (errors: 0, warnings: 4).
```

PopUp Message (on zxp007.u-aizu.ac.jp)

 lefout translation completed (errors: 0, warnings: 4). Please see the log file.

TSV.lef is exported without any errors.



---

[<== Back to Contents](#)

## 3. Modify lef file



# Modify lef file

A terminal window titled 'zxp035@zxp007:LEF\_File' with a menu bar containing 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The terminal prompt is '[zxp035@zxp007 LEF\_File]\$' and the command 'emacs TSV.lef &' has been entered, followed by a cursor. A vertical scrollbar is visible on the right side of the terminal window.

```
zxp035@zxp007:LEF_File
File Edit View Search Terminal Help
[zxp035@zxp007 LEF_File]$ emacs TSV.lef & |
```

Type **emacs TSV.lef &**



# Modify lef file

Before

```
emacs@zxp007.u-aizu.ac.jp (on zxp007.u-aizu.a _ □ ×
File Edit Options Buffers Tools Help
[Icons]
VERSION 5.7 ;[]
BUSBITCHARS "["] ;
DIVIDERCHAR "/" ;

PROPERTYDEFINITIONS
  MACRO lastSavedExtractCounter INTEGER ;
END PROPERTYDEFINITIONS

UNITS
  DATABASE MICRONS 2000 ;
END UNITS
MANUFACTURINGGRID 0.0025 ;
LAYER OVERLAP
  TYPE OVERLAP ;
END OVERLAP

LAYER active
  TYPE MASTERSLICE ;
END active
```



After

```
emacs@zxp007.u-aizu.ac.jp (on zxp007.u-aizu.a _ □ ×
File Edit Options Buffers Tools Help
[Icons]
VERSION 5.7 ;[]
BUSBITCHARS "["] ;
DIVIDERCHAR "/" ;

PROPERTYDEFINITIONS
  MACRO lastSavedExtractCounter INTEGER ;
  MACRO FE_CORE_BOX_LL_X REAL ;
  MACRO FE_CORE_BOX_UR_X REAL ;
  MACRO FE_CORE_BOX_LL_Y REAL ;
  MACRO FE_CORE_BOX_UR_Y REAL ;
END PROPERTYDEFINITIONS

UNITS
  DATABASE MICRONS 2000 ;
END UNITS
MANUFACTURINGGRID 0.0025 ;

LAYER OVERLAP
  TYPE OVERLAP ;
END OVERLAP
```

Add codes in red rectangle



# Modify lef file

Before

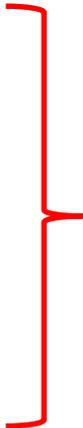
```
LAYER TM
  TYPE ROUTING ;
  DIRECTION HORIZONTAL ;
  PITCH 2 2 ;
  WIDTH 0.8 ;
  SPACING 0.8 ;
  SPACING 0.8 SAMENET ;
END TM

LAYER VDN
  TYPE CUT ;
  SPACING 6 ;
  WIDTH 6 ;
END VDN

:

LAYER VTT_E
  TYPE CUT ;
  SPACING 6 ;
  WIDTH 6 ;
END VTT_E

VIA M2_M1_via DEFAULT
  LAYER metal1 ;
  RECT -0.0675 -0.0325 0.0675 0.0325 ;
  LAYER vial ;
  RECT -0.0325 -0.0325 0.0325 0.0325 ;
  LAYER metal2 ;
  RECT -0.035 -0.0675 0.035 0.0675 ;
END M2_M1_via
```



After

```
emacs@zxp007.u-aizu.ac.jp (on zxp007.u-aizu.a _ □ ×
File Edit Options Buffers Tools Help

SPACING 0.88 ;
WIDTH 0.8 ;
END VUP

LAYER TM
  TYPE ROUTING ;
  DIRECTION HORIZONTAL ;
  PITCH 2 2 ;
  WIDTH 0.8 ;
  SPACING 0.8 ;
  SPACING 0.8 SAMENET ;
END TM

VIA M2_M1_via DEFAULT
  LAYER metal1 ;
  RECT -0.0675 -0.0325 0.0675 0.0325 ;
  LAYER vial ;
  RECT -0.0325 -0.0325 0.0325 0.0325 ;
  LAYER metal2 ;
  RECT -0.035 -0.0675 0.035 0.0675 ;
```

Delete codes in a red part



# Modify lef file

Before

```
VIA M10_M9_via DEFAULT
  LAYER metal9 ;
  RECT -0.4 -0.4 0.4 0.4 ;
  LAYER via9 ;
  RECT -0.4 -0.4 0.4 0.4 ;
  LAYER metal10 ;
  RECT -0.4 -0.4 0.4 0.4 ;
END M10_M9_via

VIA TM_M10_via DEFAULT
  LAYER metal10 ;
  RECT -0.4 -0.4 0.4 0.4 ;
  LAYER VUP ;
  RECT -0.4 -0.4 0.4 0.4 ;
  LAYER TM ;
  RECT -0.9975 -1.0 1.0025 1.0 ;
END TM_M10_via

VIA M2_M1_viaB DEFAULT
  LAYER metal1 ;
  RECT -0.0675 -0.0325 0.0675 0.0325 ;
  LAYER via1 ;
  RECT -0.0325 -0.0325 0.0325 0.0325 ;
  LAYER metal2 ;
  RECT -0.0675 -0.035 0.0675 0.035 ;
END M2_M1_viaB
```



After

```
VIA M10_M9_via DEFAULT
  LAYER metal9 ;
  RECT -0.4 -0.4 0.4 0.4 ;
  LAYER via9 ;
  RECT -0.4 -0.4 0.4 0.4 ;
  LAYER metal10 ;
  RECT -0.4 -0.4 0.4 0.4 ;
END M10_M9_via

VIA M2_M1_viaB DEFAULT
  LAYER metal1 ;
  RECT -0.0675 -0.0325 0.0675 0.0325 ;
  LAYER via1 ;
  RECT -0.0325 -0.0325 0.0325 0.0325 ;
  LAYER metal2 ;
  RECT -0.0675 -0.035 0.0675 0.035 ;
END M2_M1_viaB

VIA M2_M1_viaC DEFAULT
  LAYER metal1 ;
  RECT -0.0325 -0.0675 0.0325 0.0675 ;
  LAYER via1 ;
  RECT -0.0325 -0.0325 0.0325 0.0325 ;
  LAYER metal2 ;
  RECT -0.035 -0.0675 0.035 0.0675 ;
END M2_M1_viaC
```

Delete codes in red rectangle



# Modify lef file

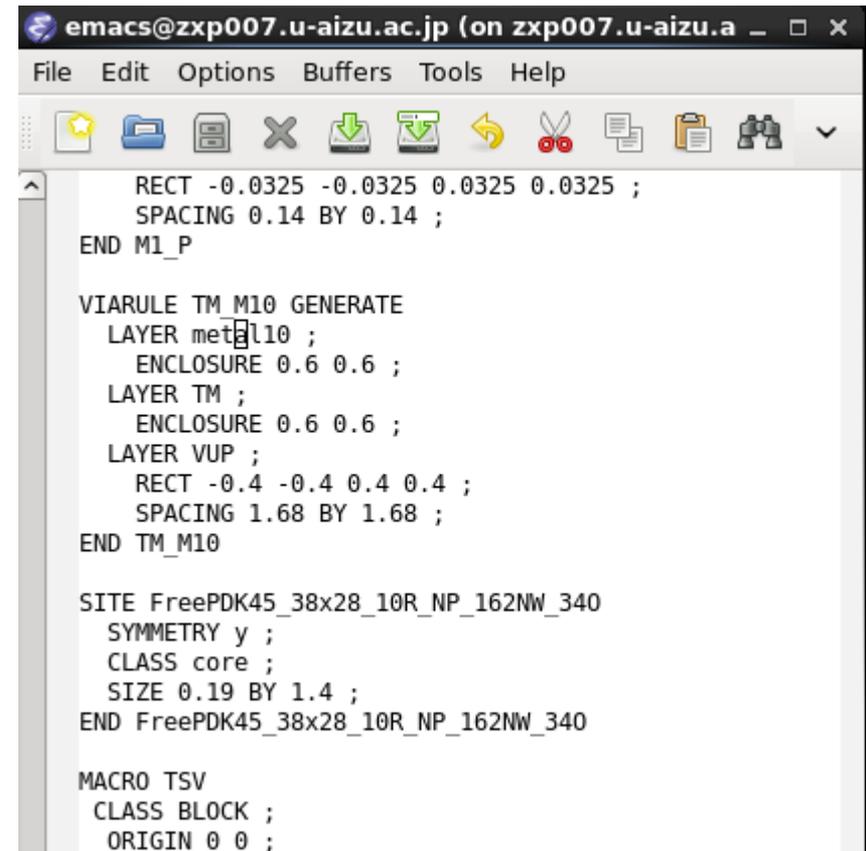
Before

```
VIARULE TM_M10 GENERATE
  LAYER metal10 ;
  ENCLOSURE 0.6 0.6 ;
  LAYER TM ;
  ENCLOSURE 0.6 0.6 ;
  LAYER VUP ;
  RECT -0.4 -0.4 0.4 0.4 ;
  SPACING 1.68 BY 1.68 ;
END TM_M10
[]
VIARULE M1_BM GENERATE
  LAYER BM ;
  ENCLOSURE 0.6 0.6 ;
  LAYER metal1 ;
  ENCLOSURE 0.1 0.1 ;
  LAYER VDN ;
  RECT -3 -3 3 3 ;
  SPACING 12 BY 12 ;
END M1_BM
:
VIA BM_D_BM_E_45
  VIARULE BM_D_BM_E ;
  CUTSIZE 6 6 ;
  LAYERS BM_D VTT_E BM_E ;
  CUTSPACING 6 6 ;
  ENCLOSURE 0.6 0.6 0.6 0.6 ;
  ROWCOL 1 1 ;
END BM_D_BM_E_45

MACRO TSV
  PROPERTY lastSavedExtractCounter 1527 ;
END TSV_
```



After



```
emacs@zxp007.u-aizu.ac.jp (on zxp007.u-aizu.a _ □ ×)
File Edit Options Buffers Tools Help
[Icons]
RECT -0.0325 -0.0325 0.0325 0.0325 ;
SPACING 0.14 BY 0.14 ;
END M1_P

VIARULE TM_M10 GENERATE
  LAYER metal10 ;
  ENCLOSURE 0.6 0.6 ;
  LAYER TM ;
  ENCLOSURE 0.6 0.6 ;
  LAYER VUP ;
  RECT -0.4 -0.4 0.4 0.4 ;
  SPACING 1.68 BY 1.68 ;
END TM_M10

SITE FreePDK45_38x28_10R_NP_162NW_340
  SYMMETRY y ;
  CLASS core ;
  SIZE 0.19 BY 1.4 ;
END FreePDK45_38x28_10R_NP_162NW_340

MACRO TSV
  CLASS BLOCK ;
  ORIGIN 0 0 ;
```

Delete codes in red rectangle



# Modify lef file

Before

```
VIARULE TM_M10 GENERATE
  LAYER metal10 ;
  ENCLOSURE 0.6 0.6 ;
  LAYER TM ;
  ENCLOSURE 0.6 0.6 ;
  LAYER VUP ;
  RECT -0.4 -0.4 0.4 0.4 ;
  SPACING 1.68 BY 1.68 ;
END TM_M10
MACRO TSV_
  PROPERTY lastSavedExtractCounter 1527 ;
END TSV_
```



After

```
VIARULE TM_M10 GENERATE
  LAYER metal10 ;
  ENCLOSURE 0.6 0.6 ;
  LAYER TM ;
  ENCLOSURE 0.6 0.6 ;
  LAYER VUP ;
  RECT -0.4 -0.4 0.4 0.4 ;
  SPACING 1.68 BY 1.68 ;
END TM_M10
SITE FreePDK45_38x28_10R_NP_162NW_340
  SYMMETRY y ;
  CLASS core ;
  SIZE 0.19 BY 1.4 ;
END FreePDK45_38x28_10R_NP_162NW_340
MACRO TSV_
  CLASS BLOCK ;
  ORIGIN 0 0 ;
  FOREIGN TSV 0 0 ;
  SIZE 4.06 BY 4.06 ;
  SYMMETRY X Y ;
  SITE FreePDK45_38x28_10R_NP_162NW_340 ;
```

Add codes in red rectangle



# Modify lef file

Before

```
CUTSPACING 6 6 ;
ENCLOSURE 0.6 0.6 0.6 0.6 ;
ROWCOL 1 1 ;
END BM_D_BM_E_45

MACRO TSV
PROPERTY lastSavedExtractCounter 1527 ;
END TSV

END LIBRARY
□
```

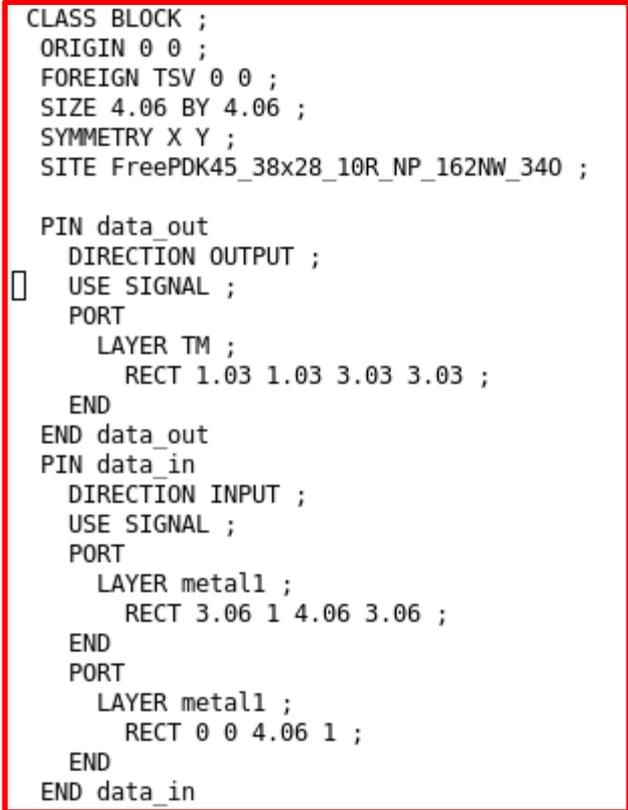


After

```
CLASS core ;
SIZE 0.19 BY 1.4 ;
END FreePDK45_38x28_10R_NP_162NW_340

MACRO TSV
CLASS BLOCK ;
ORIGIN 0 0 ;
FOREIGN TSV 0 0 ;
SIZE 4.06 BY 4.06 ;
SYMMETRY X Y ;
SITE FreePDK45_38x28_10R_NP_162NW_340 ;

PIN data_out
DIRECTION OUTPUT ;
USE SIGNAL ;
PORT
LAYER TM ;
RECT 1.03 1.03 3.03 3.03 ;
END
END data_out
PIN data_in
DIRECTION INPUT ;
USE SIGNAL ;
PORT
LAYER metall ;
RECT 3.06 1 4.06 3.06 ;
END
PORT
LAYER metall ;
RECT 0 0 4.06 1 ;
END
END data_in
```



Add codes in red rectangle



# Modify lef file

Before

```
PIN data_out
  DIRECTION OUTPUT ;
  USE SIGNAL ;
  PORT
    LAYER TM ;
    RECT 1.03 1.03 3.03 3.03 ;
  END
END data_out
PIN data_in
  DIRECTION INPUT ;
  USE SIGNAL ;
  PORT
    LAYER metall1 ;
    RECT 3.06 1 4.06 3.06 ;
  END
  PORT
    LAYER metall1 ;
    RECT 0 0 4.06 1 ;
  END
END data_in
PROPERTY lastSavedExtractCounter 1527 ;
END TSV
END LIBRARY
```



After

```
END data_in
OBS
  LAYER metall1 ;
    RECT 0 0 4.06 1.0 ;
    RECT 0 1.0 1.0 3.06 ;
    RECT 3.06 1.0 4.06 4.06 ;
    RECT 0 3.06 4.06 4.06 ;
  LAYER metall2 ;
    RECT 0 0 4.06 1.0 ;
    RECT 0 1.0 1.0 3.06 ;
    RECT 3.06 1.0 4.06 4.06 ;
    RECT 0 3.06 4.06 4.06 ;
  LAYER metall3 ;
    RECT 0 0 4.06 1.0 ;
    RECT 0 1.0 1.0 3.06 ;
    RECT 3.06 1.0 4.06 4.06 ;
    RECT 0 3.06 4.06 4.06 ;
  LAYER metall4 ;
    RECT 0 0 4.06 1.0 ;
    RECT 0 1.0 1.0 3.06 ;
    RECT 3.06 1.0 4.06 4.06 ;
    RECT 0 3.06 4.06 4.06 ;
  LAYER metall5 ;
    RECT 0 0 4.06 1.0 ;
    RECT 0 1.0 1.0 3.06 ;
    RECT 3.06 1.0 4.06 4.06 ;
    RECT 0 3.06 4.06 4.06 ;
  LAYER metall6 ;
    RECT 0 0 4.06 1.0 ;
    RECT 0 1.0 1.0 3.06 ;
    RECT 3.06 1.0 4.06 4.06 ;
    RECT 0 3.06 4.06 4.06 ;
```

Add codes in red rectangle



# Modify lef file

Before

```
LAYER metal3 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER metal4 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER metal5 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER metal6 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
PROPERTY lastSavedExtractCounter 1527 ;  
END TSV  
  
END LIBRARY  
□
```



After

```
LAYER metal6 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER metal7 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER metal8 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER metal9 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER metal10 ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
LAYER VUP ;  
  RECT 0 0 4.06 1.0 ;  
  RECT 0 1.0 1.0 3.06 ;  
  RECT 3.06 1.0 4.06 4.06 ;  
  RECT 0 3.06 4.06 4.06 ;  
END  
PROPERTY lastSavedExtractCounter 1527 ;
```

Add codes in red rectangle



# Modify lef file

Before

After

```
RECT 0 1.0 1.0 3.06 ;
RECT 3.06 1.0 4.06 4.06 ;
RECT 0 3.06 4.06 4.06 ;
LAYER metal9 ;
RECT 0 0 4.06 1.0 ;
RECT 0 1.0 1.0 3.06 ;
RECT 3.06 1.0 4.06 4.06 ;
RECT 0 3.06 4.06 4.06 ;
LAYER metal10 ;
RECT 0 0 4.06 1.0 ;
RECT 0 1.0 1.0 3.06 ;
RECT 3.06 1.0 4.06 4.06 ;
RECT 0 3.06 4.06 4.06 ;
LAYER VUP ;
RECT 0 0 4.06 1.0 ;
RECT 0 1.0 1.0 3.06 ;
RECT 3.06 1.0 4.06 4.06 ;
RECT 0 3.06 4.06 4.06 ;
END

PROPERTY lastSavedExtractCounter 1527 ;
END TSV

END LIBRARY
```



```
LAYER VUP ;
RECT 0 0 4.06 1.0 ;
RECT 0 1.0 1.0 3.06 ;
RECT 3.06 1.0 4.06 4.06 ;
RECT 0 3.06 4.06 4.06 ;
END

PROPERTY lastSavedExtractCounter 1527 ;
PROPERTY FE_CORE_BOX_LL_X 0.0 ;
PROPERTY FE_CORE_BOX_UR_X 4.06 ;
PROPERTY FE_CORE_BOX_LL_Y 0.0 ;
PROPERTY FE_CORE_BOX_UR_Y 4.06 ;
END TSV

END LIBRARY
```

Add codes in red rectangle



---

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# 4. Synthesis



# Step0: Notes

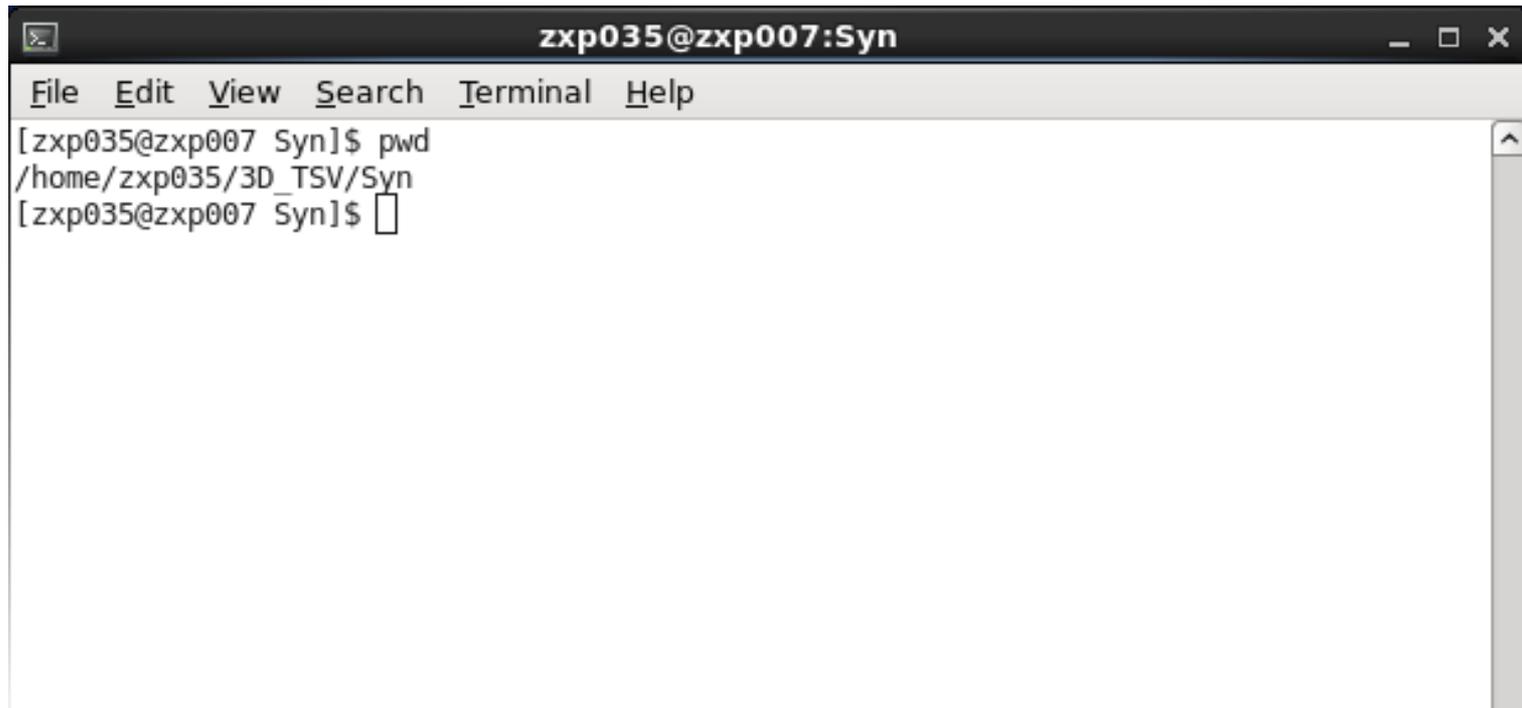
---

- In this tutorial, the synthesis step is performed using a .tcl script with a minimal use of Synopsys Design Compiler Graphic User Interface (GUI).
- To understand in details the different synthesis operations using GUI, please refer to the previously made technical report [Ref.1].



# Step1: Environment

---

A terminal window titled 'zxp035@zxp007:Syn' with standard window controls. The menu bar includes 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The terminal content shows the command 'pwd' being executed, resulting in the output '/home/zxp035/3D\_TSV/Syn'. The prompt '[zxp035@zxp007 Syn]\$' is shown again with a cursor.

```
zxp035@zxp007:Syn
File Edit View Search Terminal Help
[zxp035@zxp007 Syn]$ pwd
/home/zxp035/3D_TSV/Syn
[zxp035@zxp007 Syn]$
```

---

Go to ***/home/zxp035/3D-TSV/Syn***



## Step2: *syn\_LAFT.tcl*

---

A terminal window titled 'zxp035@zxp007:PandR' with standard window controls. The menu bar includes 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows the user is in the 'Syn' directory and has entered the command 'emacs scripts/syn\_LAFT.tcl &' followed by a cursor.

```
zxp035@zxp007:PandR  
File Edit View Search Terminal Help  
[zxp035@zxp007 Syn]$ emacs scripts/syn_LAFT.tcl & █
```

---

Type **emacs scripts/syn\_LAFT.tcl &** to see the script



# Step2: *syn\_LAFT.tcl*

```
#  
# Your design  
#  
set base_name "router_LAFT_TSV"  
set clock_name "clk"  
set clock_period 10.0  
  
#  
# Libraries  
#  
set target_library "/home/zxp035/lib/typical.db"  
set synthetic_library "dw_foundation.sldb"  
set link_library [concat "*" $target_library $synthetic_library]  
set symbol_library "generic.sdb"  
define_design_lib WORK -path ./WORK  
  
#  
# Read RTL file(s)  
#  
  
analyze -format verilog {./SRC/router_LAFT_TSV.v ./SRC/crossbar.v ./SRC/defines.v ./SRC/f  
ifo.v ./SRC/input_port.v ./SRC/matrix_arb_formultistage.v ./SRC/mux_out.v ./SRC/route.v .  
/SRC/non_minimal.v ./SRC/request_cntrl.v ./SRC/stop_go.v ./SRC/sw_alloc.v ./SRC/TSV.v}  
elaborate $base_name  
current_design $base_name  
link  
uniquify  
  
#  
# Timing  
#  
create_clock -name $clock_name -period $clock_period [find port $clock_name]  
set_clock_uncertainty 0.02 [get_clocks $clock_name]  
set_input_delay 0.1 -clock clk [remove_from_collection [all_inputs] {clk reset}]  
set_output_delay 0.1 -clock clk [all_outputs]
```



# Step2: *syn\_LAFT.tcl*

---

```
#  
# Set wire load model  
#  
set_wire_load_model -name 5K_hvratio_1_1 -library NangateOpenCellLibrary  
  
#  
# Design synthesis  
#  
compile -map_effort high  
compile -incremental_mapping -map_effort high  
  
#  
# Design report  
#  
report_qor > ./reports/Summary_report_${base_name}.txt  
report_area -hierarchy > ./reports/report_area_${base_name}.txt  
report_timing > ./reports/report_timing_${base_name}.txt  
#  
# Output  
#  
write -format verilog -hierarchy -output ./output_files/${base_name}.vnet  
write_sdc ./output_files/${base_name}.sdc  
write_file -format ddc -hierarchy -output ./DB/${base_name}.ddc  
  
# quit
```



## Step2: Run *syn\_LAFT.tcl*

---

```
zxp035@zxp007:Syn
File Edit View Search Terminal Help
[zxp035@zxp007 Syn]$ dc_shell-xg-t -f scripts/syn_LAFT.tcl
```

A terminal window titled 'zxp035@zxp007:Syn' with a menu bar containing 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows the user has entered 'dc\_shell-xg-t -f scripts/syn\_LAFT.tcl' and the cursor is at the end of the line.



# Step2: Run script

```
zxp035@zxp007:Syn
File Edit View Search Terminal Help
0:00:02 17494.8 0.00 0.0 0.0
0:00:02 17494.8 0.00 0.0 0.0
Loading db file '/home/zxp035/lib/typical.db'

Optimization Complete
-----
Warning: Design 'router_LAFT_TSV' contains 1 high-fanout nets. A fanout number of 100
0 will be used for delay calculations involving these nets. (TIM-134)
Net 'sw_allc/ol[2].spg/clock': 1547 load(s), 1 driver(s)
1
#
# Design report
#
report_qor > ./reports/Summary_report_${base_name}.txt
report_area -hierarchy > ./reports/report_area_${base_name}.txt
report_timing > ./reports/report_timing_${base_name}.txt
#
# Output
#
write -format verilog -hierarchy -output ./output_files/${base_name}.vnet
Writing verilog file '/home/zxp035/3D_TSV/Syn/output_files/router_LAFT_TSV.vnet'.
Warning: Verilog 'assign' or 'tran' statements are written out. (V0-4)
1
write_sdc ./output_files/${base_name}.sdc
1
write_file -format ddc -hierarchy -output ./DB/${base_name}.ddc
Writing ddc file './DB/router_LAFT_TSV.ddc'.
1
# quit
Information: Defining new variable 'base_name'. (CMD-041)
Information: Defining new variable 'clock_name'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
dc_shell> █
```

If red rectangles are all “1”, the script execution is succeeded



# Step3: Run GUI

```
zxp035@zxp007:Syn
File Edit View Search Terminal Help
0:00:02 17494.8 0.00 0.0 0.0
0:00:02 17494.8 0.00 0.0 0.0
Loading db file '/home/zxp035/lib/typical.db'

Optimization Complete
-----
Warning: Design 'router_LAFT_TSV' contains 1 high-fanout nets. A fanout number of 100
0 will be used for delay calculations involving these nets. (TIM-134)
Net 'sw_allc/ol[2].spg/clk': 1547 load(s), 1 driver(s)
1
#
# Design report
#
report_qor > ./reports/Summary_report_${base_name}.txt
report_area -hierarchy > ./reports/report_area_${base_name}.txt
report_timing > ./reports/report_timing_${base_name}.txt
#
# Output
#
write -format verilog -hierarchy -output ./output_files/${base_name}.vnet
Writing verilog file '/home/zxp035/3D_TSV/Syn/output_files/router_LAFT_TSV.vnet'.
Warning: Verilog 'assign' or 'tran' statements are written out. (V0-4)
1
write_sdc ./output_files/${base_name}.sdc
1
write_file -format ddc -hierarchy -output ./DB/${base_name}.ddc
Writing ddc file './DB/router_LAFT_TSV.ddc'.
1
# quit
Information: Defining new variable 'base_name'. (CMD-041)
Information: Defining new variable 'clock_name'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
dc_shell> start_gui
```

Type **start\_gui**



# Step3: Run GUI

Design Vision - TopLevel.1 (router\_LAFT\_TSV) (on zxp007.u-aizu.ac.jp)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

router\_LAFT\_TSV

Cell Name	Ref Name	Cell Path
ip0	input_port_NO...	ip0
ip1	input_port_NO...	ip1
ip2	input_port_NO...	ip2
ip3	input_port_NO...	ip3
ip4	input_port_NO...	ip4
ip5	input_port_NO...	ip5
ip6	input_port_NO...	ip6
tsv_input_u...	TSV_163	tsv_input_up0
tsv_input_d...	TSV_162	tsv_input_dow...
tsv_output...	TSV_161	tsv_output_up0
tsv_output...	TSV_160	tsv_output_do...
tsv_input_u...	TSV_159	tsv_input_up1
tsv_input_d...	TSV_158	tsv_input_dow...
tsv_output...	TSV_157	tsv_output_up1
tsv_output...	TSV_156	tsv_output_do...
tsv_input_u...	TSV_155	tsv_input_up2
tsv_input_d...	TSV_154	tsv_input_dow...
tsv_output...	TSV_153	tsv_output_up2
tsv_output...	TSV_152	tsv_output_do...
tsv_input_u...	TSV_151	tsv_input_up3
tsv_input_d...	TSV_150	tsv_input_dow...
tsv_output...	TSV_149	tsv_output_up3
tsv_output...	TSV_148	tsv_output_do...
tsv_input_u...	TSV_147	tsv_input_up4
tsv_input_d...	TSV_146	tsv_input_dow...
tsv_output...	TSV_145	tsv_output_up4
tsv_output...	TSV_144	tsv_output_do...
tsv_input_u...	TSV_143	tsv_input_up5
tsv_input_d...	TSV_142	tsv_input_dow...
tsv_output...	TSV_141	tsv_output_up5

```
Information: Defining new variable 'base_name'. (CMD-041)
Information: Defining new variable 'clock_name'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
dc_shell> start_gui
Current design is 'router_LAFT_TSV'.
Current design is 'router_LAFT_TSV'.
dc_shell>
```

Log History Options: v

Ready emacs@zxp007.u-aizu.ac.jp (on zxp007.u-aizu.ac.jp)

Click 



# Step3: Run GUI

The screenshot shows the Design Vision GUI for a router design. The main window displays a schematic diagram with two red rectangles highlighting specific components, identified as TSVs. The left pane shows a hierarchical list of cells, and the bottom pane shows a command shell with the following text:

```
Information: Defining new variable 'clock_name'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
dc_shell> start_gui
Current design is 'router_LAFT_TSV'.
Current design is 'router_LAFT_TSV'.
dc_shell>
Loading db file '/opt/vdec/Synopsys/syn_vB-2008.09/libraries/syn/generic.sdb'
```

Red rectangles are TSVs



---

[<== Back to Contents](#)

## 4. Place & Route



# Step0: Notes

---

- In this tutorial, the Place and Route step is performed using both commands and GUI.
- How to execute the commands using GUI, is explained in details in the previously made technical report [Ref.1].



# Step1: Environment

---

```
zxp035@zxp007:~$ cd /home/zxp035/3D_TSV/PandR
zxp035@zxp007:~/3D_TSV/PandR$ pwd
/home/zxp035/3D_TSV/PandR
zxp035@zxp007:~/3D_TSV/PandR$ ls
macro  script  vnet
zxp035@zxp007:~/3D_TSV/PandR$
```

---

Go to */home/zxp035/3D-TSV/PandR*



# Step1: Environment

## a- Copy the files

---

A screenshot of a terminal window titled 'zxp035@zxp007:PandR'. The window has a menu bar with 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The terminal prompt is '[zxp035@zxp007 PandR]\$' followed by the command 'cp ../LEF\_File/TSV.lef macro/' and a cursor. A vertical scrollbar is visible on the right side of the terminal area.

```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
[zxp035@zxp007 PandR]$ cp ../LEF_File/TSV.lef macro/
```

---

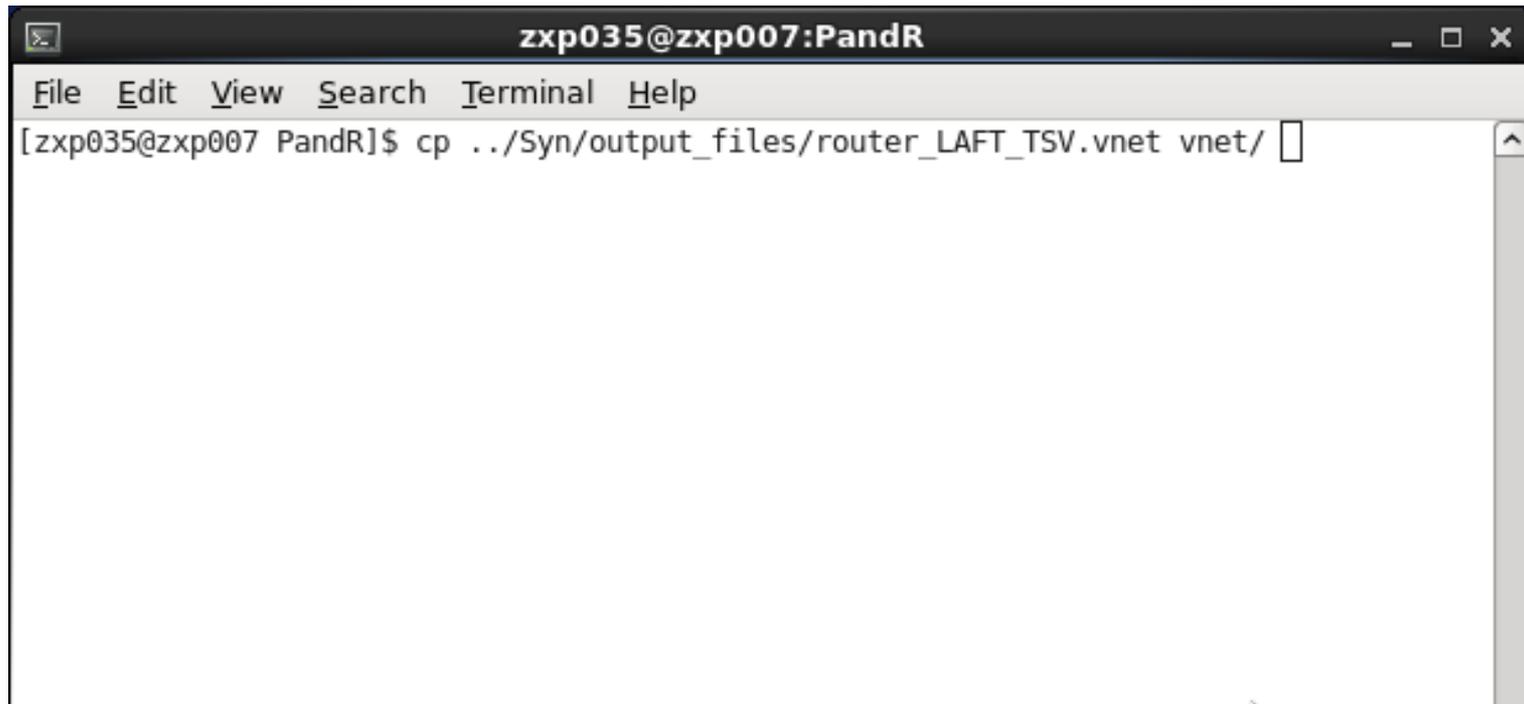
Type `cp ../LEF_File/TSV.lef macro/`



# Step1: Environment

## a- Copy the files

---

A terminal window titled 'zxp035@zxp007:PandR' with standard window controls. The menu bar includes 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows the execution of the command 'cp ../Syn/output\_files/router\_LAFT\_TSV.vnet vnet/' followed by a cursor.

```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
[zxp035@zxp007 PandR]$ cp ../Syn/output_files/router_LAFT_TSV.vnet vnet/
```

---

Type `cp ../Syn/output_files/router_LAFT.vnet vnet/`



# Step1: Environment

## b- Modify the .vnet file

---

A terminal window titled 'zxp035@zxp007:PandR' with standard window controls. The menu bar includes 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows the user has entered 'emacs vnet/router\_LAFT\_TSV.vnet &' and the cursor is at the end of the line.

```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
[zxp035@zxp007 PandR]$ emacs vnet/router_LAFT_TSV.vnet &
```

---

Type **emacs vnet/router\_LAFT\_TSV.vnet &**



# Step1: Environment

## b- Modify the vnet file

```
MUX2_X1 U398 ( .A(\fifo[0][3] ), .B(\fifo[1][3] ), .S(n711), .Z(n458) );
MUX2_X1 U399 ( .A(n458), .B(n457), .S(N15), .Z(second_item_nextport[2] ) );
endmodule
[]

module TSV_162 ( data_in, data_out );
input data_in;
output data_out;
wire data_in;
assign data_out = data_in;

endmodule

module TSV_161 ( data_in, data_out );
input data_in;

:

module TSV_1 ( data_in, data_out );
input data_in;
output data_out;
wire data_in;
assign data_out = data_in;

endmodule
[]

module TSV_0 ( data_in, data_out );
input data_in;
output data_out;
wire data_in;
assign data_out = data_in;

endmodule

module non_minimal_NOUT7_FAULTY6_5 ( xdest, ydest, zdest, xaddr, yaddr, zaddr,
```

Delete codes in a red part



# Step1: Environment

## b- Modify the vnet file

Before

```
stop_go_0 \ol[6].spg ( .clk(clk), .reset(n2), .data_sent(data_sent[6]),
    .stop_in(stop_in[6]), .blocked(blocked[6]) );
endmodule

module TSV_163 ( data_in, data_out );
    input data_in;
    output data_out;
    wire data_in;
    assign data_out = data_in;
endmodule

module input_port_NOUT7_FAULTY6_FIFO_DEPTH4_FIFO_LOG2D2_FIFO_FULL_LVL2_0 ( clk,
```



After

```
stop_go_0 \ol[6].spg ( .clk(clk), .reset(n2), .data_sent(data_sent[6]),
    .stop_in(stop_in[6]), .blocked(blocked[6]) );
endmodule

module TSV ( data_in, data_out );
    input data_in;
    output data_out;
    wire data_in;
    assign data_out = data_in;
endmodule

module input_port_NOUT7_FAULTY6_FIFO_DEPTH4_FIFO_LOG2D2_FIFO_FULL_LVL2_0 ( clk,
```

Change from TSV\_163 to TSV



# Step1: Environment

## b- Modify the vnet file

Before

After

```
input_port NOUT7_FAULTY6_FIFO_DEPTH4_FIFO_LOG2D2_FIFO_FULL_LVL2_0 ip6 (
    .clk(clk), .reset(reset), .data_in(D_data_in), .data_out(
        cbar_data_in[237:204]), .faulty_in({c_faulty_in, faulty_in}), .sw_req(
            sw_req[6]), .port_req(port_req[48:42]), .sw_grant(sw_grant[6]),
            .stop_out(D_stop_out), .xaddr(xaddr), .yaddr(yaddr), .zaddr(zaddr),
            .stop_in({alloc_stop_in, stop_in}));
    TSV_163 tsv_input_up0 ( .data_in(tsv_up_in[0]), .data_out(U_data_in[0]) );
    TSV_162 tsv_input_down0 ( .data_in(tsv_down_in[0]), .data_out(D_data_in[0])
    );
    :
    TSV_1 tsv_faulty_output_up5 ( .data_in(\faulty_out[5]), .data_out(
        tsv_faulty_up_out[5]) );
    TSV_0 tsv_faulty_output_down5 ( .data_in(\faulty_out[5]), .data_out(
        tsv_faulty_down_out[5]) );
    sw_alloc NOUT7 sw_allc ( .clk(clk), .reset(reset), .sw_req(sw_req),
        .stop_in({alloc_stop_in, stop_in}), .data_sent(data_sent), .tail_sent(
            {tsv_down_out[0], tsv_up_out[0], data_out[136], data_out[102],
            data_out[68], data_out[34], data_out[0]}), .port_req(port_req),
            .grant_out(sw_grant), .sw_cntrl(sw_cntrl) );
    crossbar NOUT7_NIN7_WIDTH34 cbar ( .clk(clk), .reset(reset), .cntrl(sw_cntrl),
    .data_in(cbar_data_in), .data_out({cbar_data_out, data_out}));
endmodule
```



```
input_port NOUT7_FAULTY6_FIFO_DEPTH4_FIFO_LOG2D2_FIFO_FULL_LVL2_0 ip6 (
    .clk(clk), .reset(reset), .data_in(D_data_in), .data_out(
        cbar_data_in[237:204]), .faulty_in({c_faulty_in, faulty_in}), .sw_req(
            sw_req[6]), .port_req(port_req[48:42]), .sw_grant(sw_grant[6]),
            .stop_out(D_stop_out), .xaddr(xaddr), .yaddr(yaddr), .zaddr(zaddr),
            .stop_in({alloc_stop_in, stop_in}));
    TSV tsv_input_up0 ( .data_in(tsv_up_in[0]), .data_out(U_data_in[0]) );
    TSV tsv_input_down0 ( .data_in(tsv_down_in[0]), .data_out(D_data_in[0])
    );
    :
    TSV tsv_faulty_output_up5 ( .data_in(\faulty_out[5]), .data_out(
        tsv_faulty_up_out[5]) );
    TSV tsv_faulty_output_down5 ( .data_in(\faulty_out[5]), .data_out(
        tsv_faulty_down_out[5]) );
    sw_alloc NOUT7 sw_allc ( .clk(clk), .reset(reset), .sw_req(sw_req),
        .stop_in({alloc_stop_in, stop_in}), .data_sent(data_sent), .tail_sent(
            {tsv_down_out[0], tsv_up_out[0], data_out[136], data_out[102],
            data_out[68], data_out[34], data_out[0]}), .port_req(port_req),
            .grant_out(sw_grant), .sw_cntrl(sw_cntrl) );
    crossbar NOUT7_NIN7_WIDTH34 cbar ( .clk(clk), .reset(reset), .cntrl(sw_cntrl),
    .data_in(cbar_data_in), .data_out({cbar_data_out, data_out}));
endmodule
```

Change from TSV\_\* to TSV



# Step2: Run SoC Encounter

---

A terminal window titled 'zxp035@zxp007:PandR' with standard window controls (minimize, maximize, close). The menu bar includes 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The command prompt shows '[zxp035@zxp007 PandR]\$ velocity' followed by a cursor. A vertical scrollbar is visible on the right side of the terminal area.

```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
[zxp035@zxp007 PandR]$ velocity
```

---

Type **velocity** to start SoC Encounter

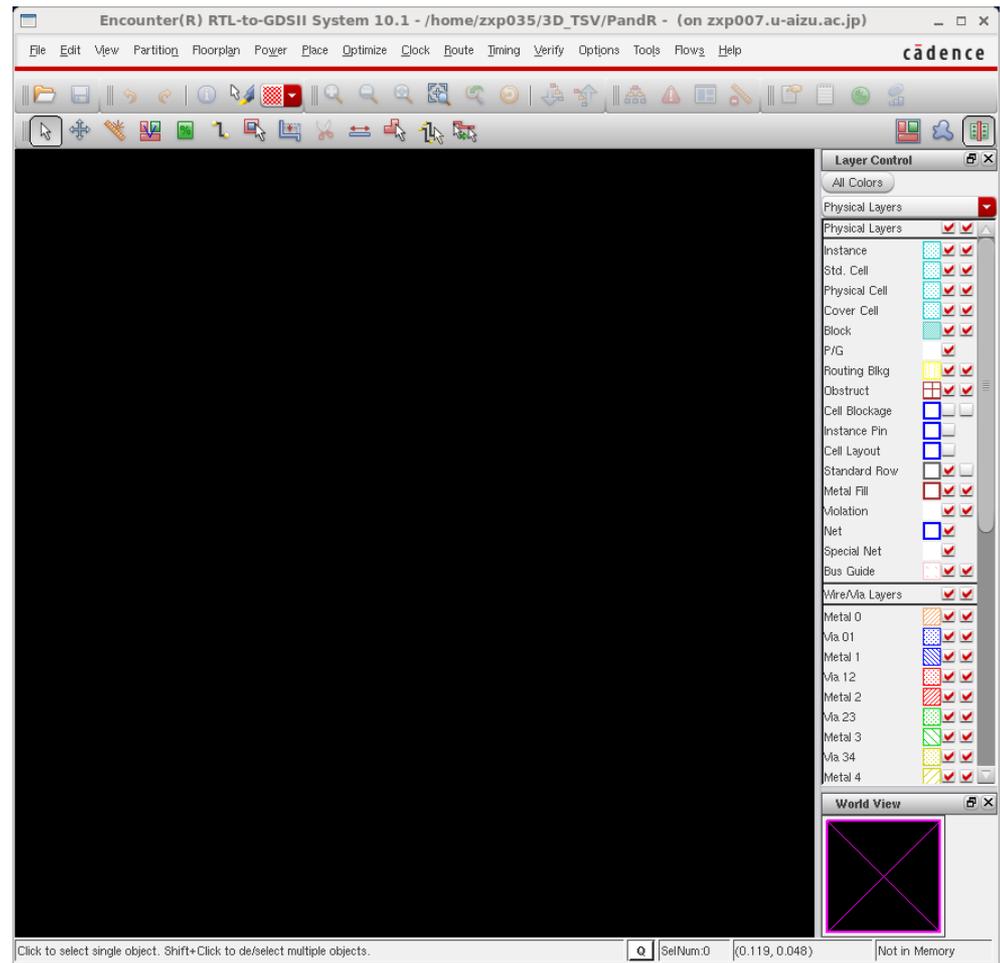


# Step2: Run SoC Encounter

```
zxp035@zxp007:~$ velocity
[~$ velocity
Checking out Encounter license ...
Encounter_Digital_Impl_Sys_XL_10.1 license checkout succeeded.
You can run 2 CPU jobs with the base license that is currently checked out.
If required, use the setMultiCpuUsage command to enable multi-CPU processing.
This Encounter release has been compiled with OA version 22.04-p001.

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@(#)CDS: Encounter v10.10-p003_1 (32bit) 12/09/2010 19:05 (Linux 2.6)
@(#)CDS: NanoRoute v10.10-p002 NR101202-1141/USR66-UB (database version 2.30, 109.2.1)
{superthreading v1.15}
@(#)CDS: CeltIC v10.10-p001_1 (32bit) 11/30/2010 03:36:40 (Linux 2.6.9-89.0.19.ELsmp)
@(#)CDS: AAE 10.10-p001 (32bit) 12/09/2010 (Linux 2.6.9-89.0.19.ELsmp)
@(#)CDS: CTE 10.10-p001_1 (32bit) Nov 29 2010 23:33:07 (Linux 2.6.9-89.0.19.ELsmp)
@(#)CDS: CPE v10.10-p003
--- Starting "Encounter v10.10-p003_1" on Wed May 27 12:45:28 2015 (mem=42.8M) ---
--- Running on zxp007.u-aizu.ac.jp (x86_64 w/Linux 2.6.32-504.1.3.el6.x86_64) ---
This version was compiled on Thu Dec 9 19:05:34 PST 2010.
Set DBUPerIGU to 1000.
Set net toggle Scale Factor to 1.00
Set Shrink Factor to 1.00000
velocity i>
```



Welcome screen of SoC Encounter.

The CUI is on the left side and the GUI is in the right side.



# Step3: Import Design

```
zxp035@zxp007:~$ velocity
Checking out Encounter license ...
Encounter_Digital_Impl_Sys_XL 10.1 license checkout succeeded.
You can run 2 CPU jobs with the base license that is currently checked out.
If required, use the setMultiCpuUsage command to enable multi-CPU processing.
This Encounter release has been compiled with OA version 22.04-p001.

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* San Jose, CA 95134, USA *
* *
*****

@(#)CDS: Encounter v10.10-p003 1 (32bit) 12/09/2010 19:05 (Linux 2.6)
@(#)CDS: NanoRoute v10.10-p002 NR101202-1141/USR66-UB (database version 2.30, 109.2.1)
) {superthreading v1.15}
@(#)CDS: CeltIC v10.10-p001 1 (32bit) 11/30/2010 03:36:40 (Linux 2.6.9-89.0.19.ELsmp)
@(#)CDS: AAE 10.10-p001 (32bit) 12/09/2010 (Linux 2.6.9-89.0.19.ELsmp)
@(#)CDS: CTE 10.10-p001 1 (32bit) Nov 29 2010 23:33:07 (Linux 2.6.9-89.0.19.ELsmp)
@(#)CDS: CPE v10.10-p003
--- Starting "Encounter v10.10-p003 1" on Wed May 27 12:45:28 2015 (mem=42.8M) ---
--- Running on zxp007.u-aizu.ac.jp (x86_64 w/Linux 2.6.32-504.1.3.el6.x86_64) ---
This version was compiled on Thu Dec 3 19:05:34 PST 2010.
Set DBUPerIGU to 1000.
Set net toggle Scale Factor to 1.00
Set Shrink Factor to 1.00000
velocity 1>
```

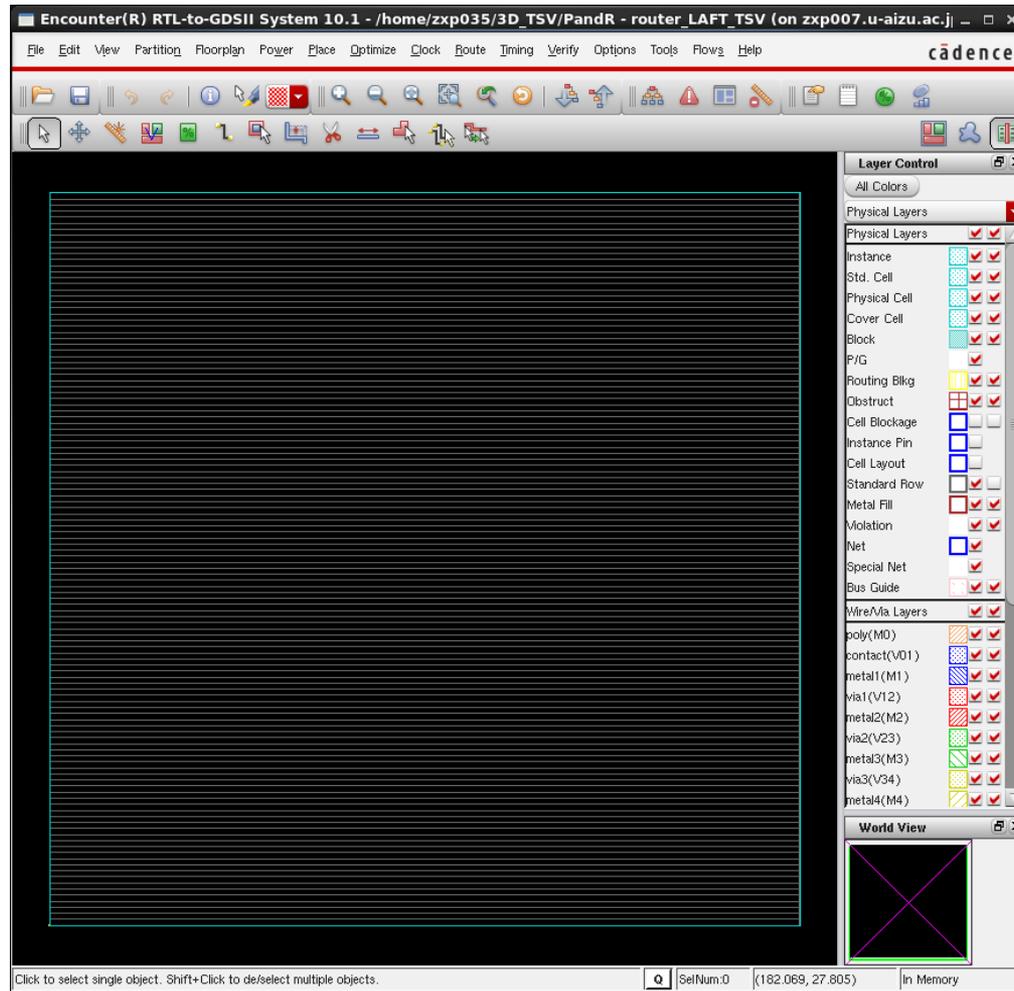
```
#
# Step 1: Setup (File --> Import Design)
#
setUIVar rda_Input ui_netlist vnet/router_LAFT_TSV.vnet
setUIVar rda_Input ui_timingcon_file ../Syn/output_files/router_LAFT_TSV.sdc
setUIVar rda_Input ui_topcell router_LAFT_TSV
setUIVar rda_Input ui_leffile {macro/TSV.lef /home/zxp035/lib/NangateOpenCellLibrary.lef}
setUIVar rda_Input ui_timelib {/home/zxp035/lib/typical.lib macro/TSV.lib}

setUIVar rda_Input ui_pwrnet VDD
setUIVar rda_Input ui_gndnet VSS
setUIVar rda_Input ui_cts_cell_list {CLKBUF_X1 CLKBUF_X2 CLKBUF_X3}
commitConfig
```

Execute the commands on the right hand in the CUI line by line to **import** the previously synthesized design



# Step3: Import Design



The initial chip layout **after importing** the design



# Step4: SoC Floorplan and macro

```
zxp035@zxp007:~$ cat floorplan.tcl
File Edit View Search Terminal Help
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers: BUF_X1 BUF_X2 BUF_X4 BUF_X8 BUF_X16 BUF_X32 CLKBUF_X1 CLKBUF_X2 CLKBUF_X3
Total number of usable buffers: 9
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters: INV_X1 INV_X2 INV_X4 INV_X8 INV_X16 INV_X32
Total number of usable inverters: 6
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells:
Total number of identified usable delay cells: 0
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0
No delay cells were detected in the set of buffers. Buffers will be used to fix hold violations.
*info: set bottom ioPad orient R0
**WARN: (ENCRM-128): Total 1 bad sites (size is not multiple of H/V pitch).
Horizontal Layer M1 offset = 190 (guessed)
Vertical Layer M2 offset = 190 (derived)
Suggestion: specify LAYER OFFSET in LEF file
Reason: hard to extract LAYER OFFSET from standard cells
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Set Input Pin Transition Delay as 0.1 ps.
PreRoute Cap Scale Factor : 1.00
PreRoute Res Scale Factor : 1.00
PostRoute Cap Scale Factor : 1.00
PostRoute Res Scale Factor : 1.00
PostRoute XCap Scale Factor : 1.00

PreRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)]
PreRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)]
PostRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)]
PostRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)]
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing libraries, unit of 1pf will be used. Use setLibraryUnit command to set consistent capacitive load unit for the design.
**WARN: (ENCK-7003): Command "addCTSCellList" is obsolete. Use "specifyClockTree -update (AutoCTSRootPin clkname Buffer bufferList ...)" as an alternative. The obsolete command still works in this release, but to avoid this warning and to ensure compatibility with future releases, remove "addCTSCellList" from your script.
Set CTS cells: CLKBUF_X1 CLKBUF_X2 CLKBUF_X3
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing libraries, unit of 1pf will be used. Use setLibraryUnit command to set consistent capacitive load unit for the design.
0
velocity 10> velocity 10> █
```

```
floorPlan -s 300 300 15 15 15 15
#set halo#
addHaloToBlock 0.5 0.5 0.5 0.5 -allBlock

createRouteBlk -box 0 0 380 65 -layer 11
createRouteBlk -box 0 65 65 265 -layer 11
createRouteBlk -box 265 65 380 265 -layer 11
createRouteBlk -box 0 265 380 380 -layer 11

#place macro
placeInstance tsv_input_up0 75 75 R0
placeInstance tsv_input_up1 75 90 R0

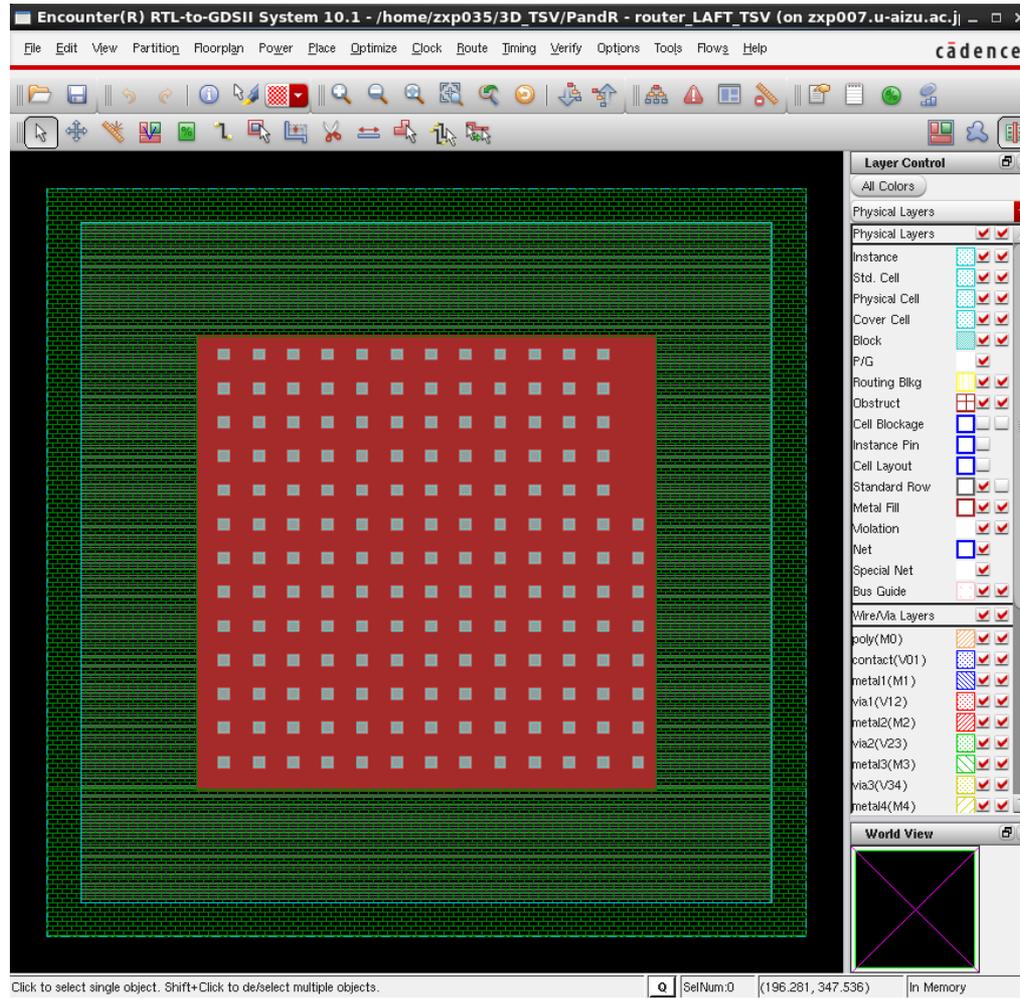
:
placeInstance tsv_faulty_output_down4 255 120 R0
placeInstance tsv_faulty_input_up5 255 135 R0
placeInstance tsv_faulty_input_down5 255 150 R0
placeInstance tsv_faulty_output_up5 255 165 R0
placeInstance tsv_faulty_output_down5 255 180 R0

createObstruct 65 65 265 265
```

Execute the commands on the right hand in the CUI line by line to set floorplan and macro locations



# Step4: SoC Floorplan and macro



Chip layout after Floorplan and macro placement



# Step5: Power ring

```
zxp035@zxp007:~$ pandr
File Edit View Search Terminal Help
X2 CLKBUF_X3
Total number of usable buffers: 9
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters: INV_X1 INV_X2 INV_X4 INV_X8 INV_X16 INV_X32
Total number of usable inverters: 6
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells:
Total number of identified usable delay cells: 0
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0
No delay cells were detected in the set of buffers. Buffers will be used to fix hold
violations.
*info: set bottom ioPad orient R0
**WARN: (ENCRM-128): Total 1 bad sites (size is not multiple of H/V pitch).
Horizontal Layer M1 offset = 190 (guessed)
Vertical Layer M2 offset = 190 (derived)
Suggestion: specify LAYER OFFSET in LEF file
Reason: hard to extract LAYER OFFSET from standard cells
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Set Input Pin Transition Delay as 0.1 ps.
PreRoute Cap Scale Factor : 1.00
PreRoute Res Scale Factor : 1.00
PostRoute Cap Scale Factor : 1.00
PostRoute Res Scale Factor : 1.00
PostRoute XCap Scale Factor : 1.00

PreRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)
]
PreRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)
]
PostRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)
]
PostRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)
]
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing lib
raries, unit of 1pf will be used. Use setLibraryUnit command to set consistent capaci
tive load unit for the design.
**WARN: (ENCK-7003): Command "addCTSCellList" is obsolete. Use "specifyClockTree -
update {AutoCTSRootPin clkname Buffer bufferlist ...}" as an alternative. The obsole
te command still works in this release, but to avoid this warning and to ensure compat
ibility with future releases, remove "addCTSCellList" from your script.
Set CTS cells: CLKBUF_X1 CLKBUF_X2 CLKBUF_X3
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing lib
raries, unit of 1pf will be used. Use setLibraryUnit command to set consistent capaci
tive load unit for the design.
Adjusting Core to Left to: 15.0100. Core to Bottom to: 15.0100.
**WARN: (ENCRM-128): Total 1 bad sites (size is not multiple of H/V pitch).
Horizontal Layer M1 offset = 190 (guessed)
Vertical Layer M2 offset = 190 (derived)
Suggestion: specify LAYER OFFSET in LEF file
Reason: hard to extract LAYER OFFSET from standard cells
**WARN: (ENCFP-325): After proportional resize, all pre-routed wires will be remov
ed.
velocity 1>
```

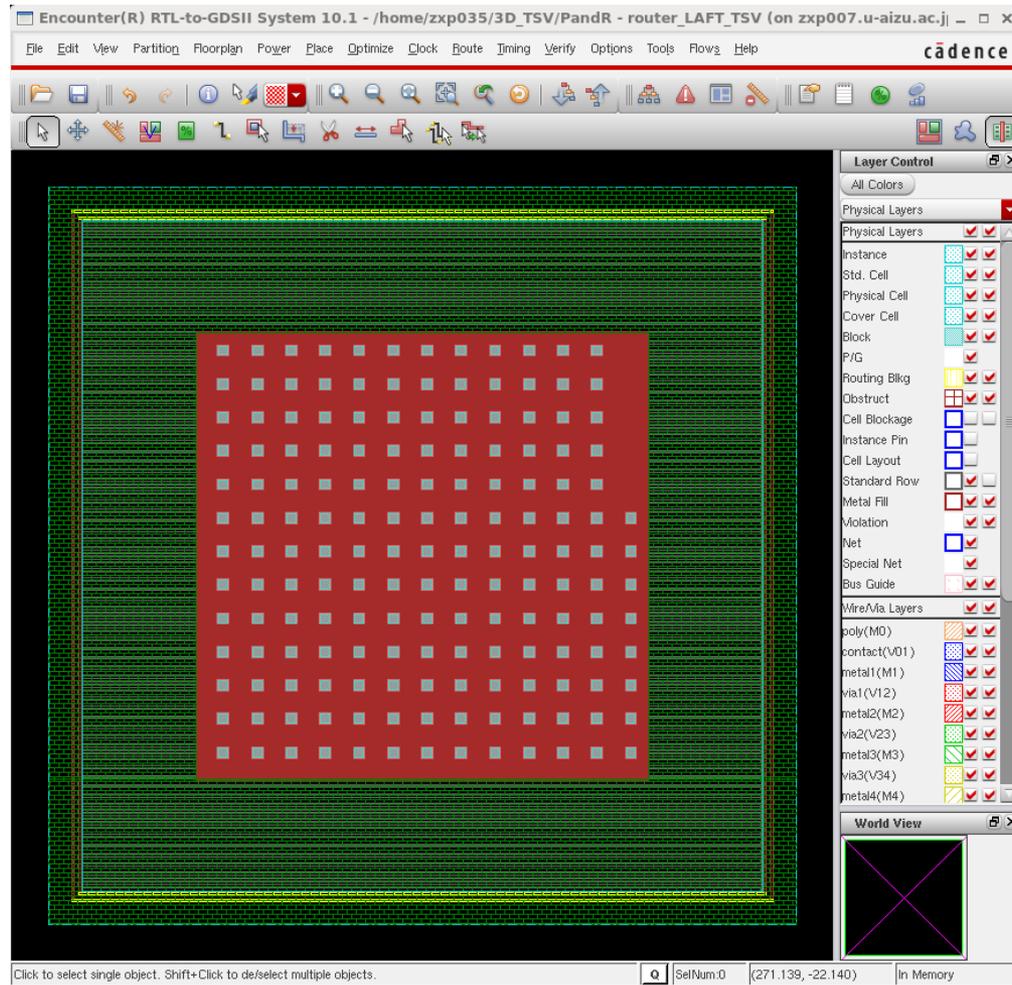
```
#
# Step 3: Power ring (Power --> Power Planning --> Add Ring)
#
createPGPin VDD -net VDD
createPGPin VSS -net VSS

addRing -nets {VSS VDD} -type core_rings \
  -spacing_top 2 -spacing_bottom 2 -spacing_right 2 -spacing_left 2 \
  -width_top 1 -width_bottom 1 -width_right 1 -width_left 1 \
  -around_core -jog_distance 0.095 -threshold 0.095 \
  -layer_top metal10 -layer_bottom metal10 -layer_right metal9 \
  -layer_left metal9 \
  -stacked_via_top_layer metal10 -stacked_via_bottom_layer metal1
```

Execute the commands on the right hand in the CUI line by line  
to add the power ring



# Step5: Power ring



Chip layout after adding the power ring



# Step6: Power Stripe

```
zxp035@zxp007:~$ pandr
File Edit View Search Terminal Help
No delay cells were detected in the set of buffers. Buffers will be used to fix hold
violations.
*info: set bottom ioPad orient R0
**WARN: (ENCRM-128): Total 1 bad sites (size is not multiple of H/V pitch).
Horizontal Layer M1 offset = 190 (guessed)
Vertical Layer M2 offset = 190 (derived)
Suggestion: specify LAYER OFFSET in LEF file
Reason: hard to extract LAYER OFFSET from standard cells
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Set Input Pin Transition Delay as 0.1 ps.
PreRoute Cap Scale Factor : 1.00
PreRoute Res Scale Factor : 1.00
PostRoute Cap Scale Factor : 1.00
PostRoute Res Scale Factor : 1.00
PostRoute XCap Scale Factor : 1.00

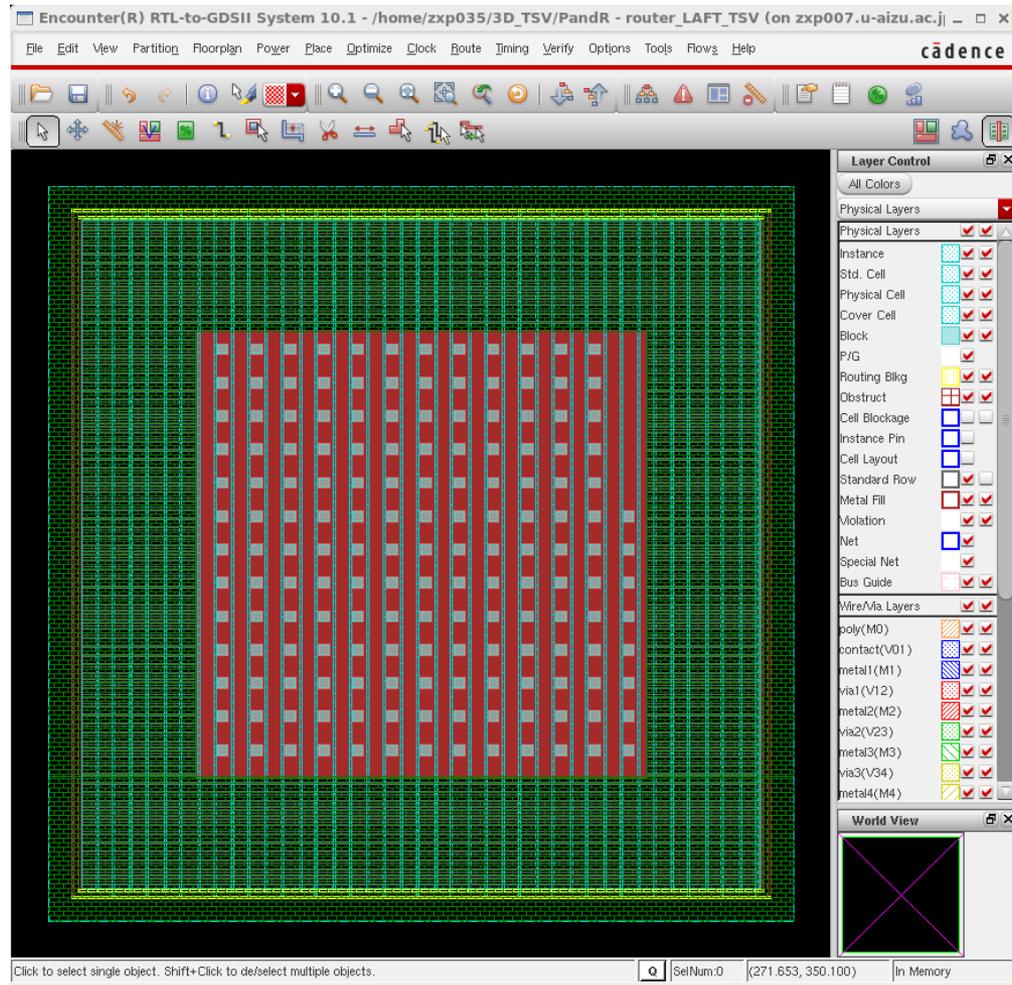
PreRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)
]
PreRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)
]
PostRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)
]
PostRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)
]
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing lib
raries, unit of IpF will be used. Use setLibraryUnit command to set consistent capaci
tive load unit for the design.
**WARN: (ENCK-7003): Command "addCTSCellList" is obsolete. Use "specifyClockTree -
update {AutoCTSRootPin clkname Buffer bufferlist ...}" as an alternative. The obsolete
command still works in this release, but to avoid this warning and to ensure compat
ibility with future releases, remove "addCTSCellList" from your script.
Set CTS cells: CLKBUF_X1 CLKBUF_X2 CLKBUF_X3
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing lib
raries, unit of IpF will be used. Use setLibraryUnit command to set consistent capaci
tive load unit for the design.
Adjusting Core to Left to: 15.0100. Core to Bottom to: 15.0100.
**WARN: (ENCRM-128): Total 1 bad sites (size is not multiple of H/V pitch).
Horizontal Layer M1 offset = 190 (guessed)
Vertical Layer M2 offset = 190 (derived)
Suggestion: specify LAYER OFFSET in LEF file
Reason: hard to extract LAYER OFFSET from standard cells
**WARN: (ENCFP-325): After proportional resize, all pre-routed wires will be remov
ed.
velocity 1> createPGPin VDD -net VDD
velocity 2> createPGPin VSS -net VSS
velocity 3> addRing -nets {VSS VDD} -type core_rings \
+ -spacing_top 2 -spacing_bottom 2 -spacing_right 2 -spacing_left 2 \
+ -width_top 1 -width_bottom 1 -width_right 1 -width_left 1 \
+ -around_core -jog_distance 0.095 -threshold 0.095 \
+ -layer_top metal10 -layer_bottom metal10 -layer_right metal9 \
+ -layer_left metal9 \
+ -stacked_via_top_layer metal10 -stacked_via_bottom_layer metal1
The power planner created 8 wires.
*** Ending Ring Generation (totcpu=0:00:00.0, real=0:00:00.0, mem=244.1M) ***
velocity 4>
```

```
#
# Step 4: Power stripe (Power --> Power Planning --> Add Stripe)
#
addStripe -nets {VSS VDD} -layer metal8 -width 1 -spacing 6 \
-block_ring_top_layer_limit metal9 -block_ring_bottom_layer_limit metal7 \
-padcore_ring_top_layer_limit metal9 -padcore_ring_bottom_layer_limit metal7 \
-stacked_via_top_layer metal10 -stacked_via_bottom_layer metal1 \
-set_to_set_distance 15 -xleft_offset 6 -merge_stripes_value 0.095 \
-max_same_layer_jog_length 1.6
```

Execute the commands on the right hand in the CUI line by line  
to add power stripe



# Step6: Power Stripe



Chip layout after adding the power stripe



# Step7: Power Routing

```
zxp035@zxp007:~$ pandr
File Edit View Search Terminal Help
PostRoute Res Scale Factor : 1.00
PostRoute XCap Scale Factor : 1.00

PreRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)
]
PreRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)
]
PostRoute Clock Cap Scale Factor : 1.00 [Derived from postRoute_cap (effortLevel low)
]
PostRoute Clock Res Scale Factor : 1.00 [Derived from postRoute_res (effortLevel low)
]
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing lib
raries, unit of lpf will be used. Use setLibraryUnit command to set consistent capaci
tive load unit for the design.
**WARN: (ENCK-7003): Command "addCTSCellList" is obsolete. Use "specifyClockTree -
update {AutoCTSRootPin clkname Buffer bufferlist ...}" as an alternative. The obsole
te command still works in this release, but to avoid this warning and to ensure compat
ibility with future releases, remove "addCTSCellList" from your script.
Set CTS cells: CLKBUF_X1 CLKBUF_X2 CLKBUF_X3
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing lib
raries, unit of lpf will be used. Use setLibraryUnit command to set consistent capaci
tive load unit for the design.
Adjusting Core to Left to: 15.0100. Core to Bottom to: 15.0100.
**WARN: (ENCRM-128): Total 1 bad sites (size is not multiple of H/V pitch).
Horizontal Layer M1 offset = 190 (guessed)
Vertical Layer M2 offset = 190 (derived)
Suggestion: specify LAYER OFFSET in LEF file
Reason: hard to extract LAYER OFFSET from standard cells
**WARN: (ENCFF-325): After proportional resize, all pre-routed wires will be remov
ed.
velocity 1> createPGPin VDD -net VDD
velocity 2> createPGPin VSS -net VSS
velocity 3> addRing -nets {VSS VDD} -type core_rings \
+ -spacing_top 2 -spacing_bottom 2 -spacing_right 2 -spacing_left 2 \
+ -width_top 1 -width_bottom 1 -width_right 1 -width_left 1 \
+ -around_core -jog_distance 0.095 -threshold 0.095 \
+ -layer_top metal10 -layer_bottom metal10 -layer_right metal9 \
+ -layer_left metal9 \
+ -stacked_via_top_layer metal10 -stacked_via_bottom_layer metal1
]

The power planner created 8 wires.
*** Ending Ring Generation (totcpu=0:00:00.0, real=0:00:00.0, mem=344.1M) ***
velocity 4> addStripe -nets {VSS VDD} -layer metal8 -width 1 -spacing 6 \
+ -block_ring_top_layer_limit metal9 -block_ring_bottom_layer_limit metal7 \
+ -padcore_ring_top_layer_limit metal9 -padcore_ring_bottom_layer_limit metal7 \
+ -stacked_via_top_layer metal10 -stacked_via_bottom_layer metal1 \
+ -set_to_set_distance 15 -xleft_offset 6 -merge_stripes_value 0.095 \
+ -max_same_layer_jog_length 1.6
**WARN: (ENCFF-2008): AddStripe option remove_floating_stripe_over_block is ON so
all fragmented stripes within a block will be removed.
To turn OFF, setAddStripeOption remove_floating_stripe_over_block 0.

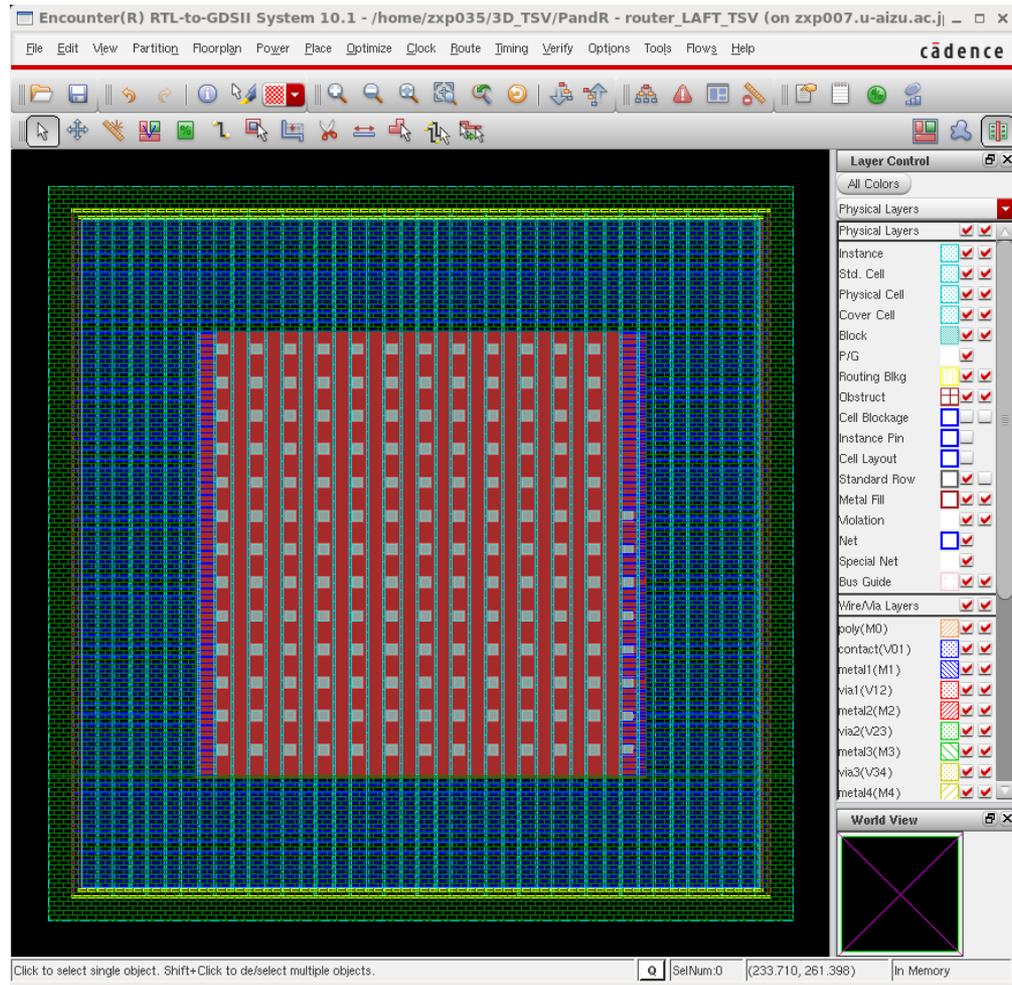
Starting stripe generation
Non-Default setAddStripeOption Settings :
NONE
Stripe generation is complete; vias are now being generated.
The power planner created 40 wires.
velocity 5>
```

```
#
# Step 5: Power route (Route --> Special Router)
#
sroute -nets {VSS VDD} -layerChangeRange {1 10} \
- connect { blockPin padPin padRing corePin floatingStripe } \
- blockPinTarget { nearestRingStripe nearestTarget } \
- padPinPortConnect { allPort oneGeom } \
- checkAlignedSecondaryPin 1 -blockPin useLef -allowJogging 1 \
- crossoverViaBottomLayer 1 -allowLayerChange 1 -targetViaTopLayer 10 \
- crossoverViaTopLayer 10 -targetViaBottomLayer 1
```

Execute the commands on the right hand in the CUI line by line to make special route



# Step7: Power Routing



Chip layout after making the special route



# Step8: Placement

```
zxp035@zxp007:~$ pandr
File Edit View Search Terminal Help
**WARN: (ENC SR-468): No core cells defined in COMPONENTS section
and/or No core cells defined in SPECIALNETS VSS
**WARN: (ENC SR-468): No core cells defined in COMPONENTS section
and/or No core cells defined in SPECIALNETS VSS
CPU time for FollowPin 0 seconds
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
**WARN: LAYER vial, same net spacing is larger than different net spacing!
**WARN: LAYER via2, same net spacing is larger than different net spacing!
**WARN: LAYER via3, same net spacing is larger than different net spacing!
Number of IO ports routed: 0
Number of Block ports routed: 0
Number of Stripe ports routed: 0
Number of Core ports routed: 716
Number of Pad ports routed: 0
Number of Power Bump ports routed: 0
Number of Followpin connections: 358
End power routing: cpu: 0:00:00, real: 0:00:00, peak: 493.00 megs.

Begin updating DB with routing results ...
Updating DB with 65 via definition ...Extracting standard cell pins and blockage ...
...
Pin and blockage extraction finished

sroute post-processing starts at Wed May 27 13:06:53 2015
The viaGen is rebuilding shadow vias for net VSS.
sroute post-processing ends at Wed May 27 13:06:53 2015

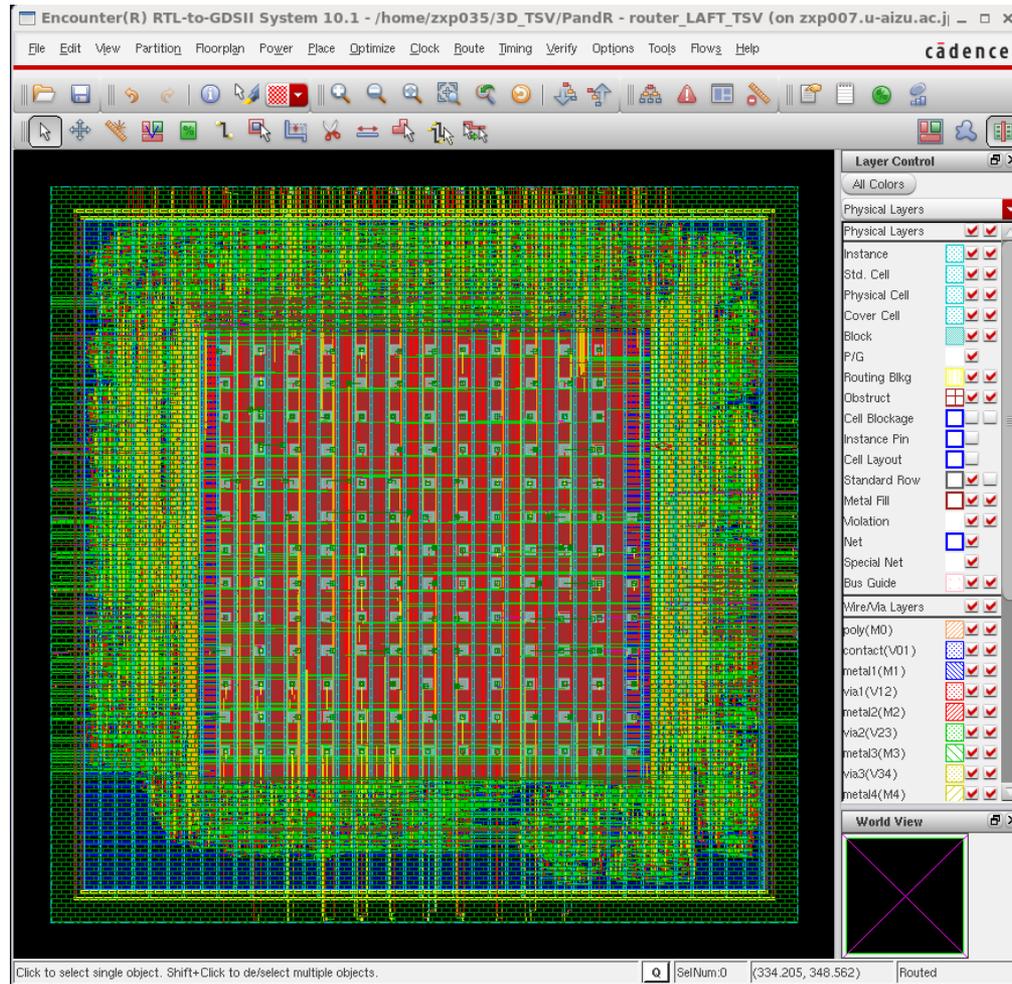
sroute post-processing starts at Wed May 27 13:06:53 2015
The viaGen is rebuilding shadow vias for net VDD.
sroute post-processing ends at Wed May 27 13:06:53 2015
sroute: Total CPU time used = 0:0:0
sroute: Total Real time used = 0:0:0
sroute: Total Memory used = 6.36 megs
sroute: Total Peak Memory used = 250.96 megs
velocity 6>
```

```
#
# Step 6: Placement (Place --> Standard Cell)
#
placeDesign -prePlaceOpt
```

Execute the commands on the right hand in the CUI line by line to place the standard cells



# Step8: Placement



Chip layout after placing the standard cells



# Step9: Optimization

```
zxp035@zxp007:~$ velocity >
File Edit View Search Terminal Help
-6: 0 0.00% 6 0.01%
-5: 0 0.00% 7 0.02%
-4: 0 0.00% 37 0.09%
-3: 3 0.01% 79 0.19%
-2: 8 0.02% 118 0.28%
-1: 27 0.06% 257 0.60%
-----
0: 127 0.30% 486 1.14%
1: 352 0.82% 897 2.10%
2: 227 0.53% 554 1.30%
3: 203 0.47% 566 1.33%
4: 391 0.91% 954 2.24%
5: 513 1.20% 970 2.28%
6: 722 1.69% 1060 2.49%
7: 1177 2.75% 1136 2.66%
8: 1773 4.15% 1330 3.12%
9: 2023 4.73% 1562 3.66%
10: 2335 5.46% 1614 3.79%
11: 2682 6.27% 1861 4.37%
12: 3445 8.05% 3388 7.95%
13: 3337 7.80% 4518 10.60%
14: 3854 9.01% 1845 4.33%
15: 5329 12.46% 2853 6.69%
16: 3324 7.77% 1198 2.81%
17: 1307 3.06% 483 1.13%
18: 979 2.29% 597 1.40%
19: 1079 2.52% 643 1.51%
20: 7554 17.66% 13611 31.93%

*** Completed Phase 1 route (0:00:00.5 282.7M) ***

Total length: 2.569e+05um, number of vias: 81568
M1(H) length: 5.595e+03um, number of vias: 39631
M2(V) length: 8.589e+04um, number of vias: 31681
M3(H) length: 8.904e+04um, number of vias: 5578
M4(V) length: 3.414e+04um, number of vias: 1951
M5(H) length: 1.757e+04um, number of vias: 1279
M6(V) length: 1.917e+04um, number of vias: 426
M7(H) length: 6.145e+02um, number of vias: 385
M8(V) length: 3.170e+03um, number of vias: 258
M9(H) length: 2.047e+02um, number of vias: 211
M10(V) length: 1.096e+03um, number of vias: 168
M11(H) length: 3.887e+02um
*** Completed Phase 2 route (0:00:00.4 282.7M) ***

*** Finished all Phases (cpu=0:00:00.9 mem=282.7M) ***
Peak Memory Usage was 286.7M
*** Finished trialRoute (cpu=0:00:00.9 mem=282.7M) ***

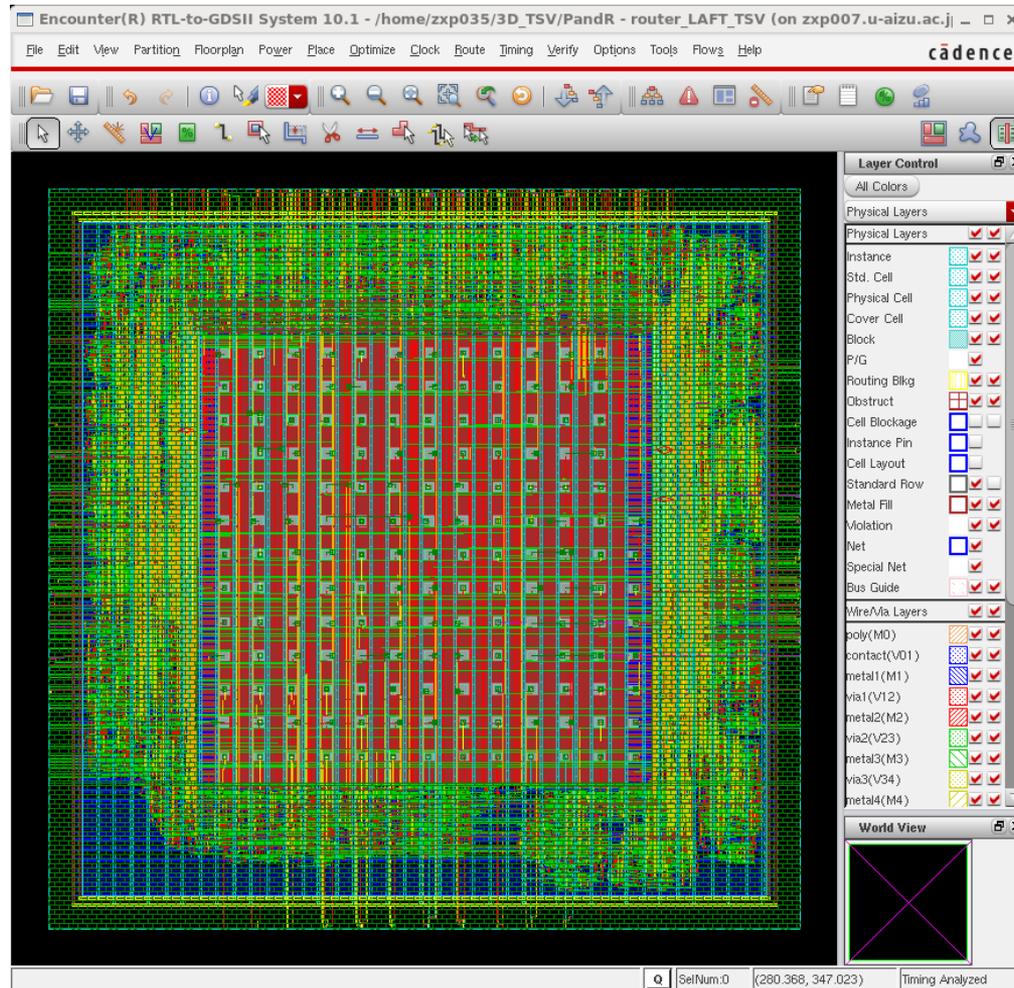
End of congRepair (cpu=0:00:05.4, real=0:00:06.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:24
***** Total real time 0:0:24
**placeDesign ... cpu = 0:0:24, real = 0:0:24, mem = 282.7M **
velocity > velocity >
```

```
#
# Step 7: Optimization (preCTS) (Optimize --> Optimize Design)
#
optDesign -preCTS
```

Execute the commands on the right hand in the CUI line by line to perform the **Pre-clock synthesis optimization**



# Step9: Optimization



Chip layout after the **Pre-clock synthesis optimization**



# Step10: Clock Tree

```
zxp035@zxp007:~$ velocity
File Edit View Search Terminal Help
-6: 0 0.00% 6 0.01%
-5: 0 0.00% 7 0.02%
-4: 0 0.00% 37 0.09%
-3: 3 0.01% 79 0.19%
-2: 8 0.02% 118 0.28%
-1: 27 0.06% 257 0.60%
-----
0: 127 0.30% 486 1.14%
1: 352 0.82% 897 2.10%
2: 227 0.53% 554 1.30%
3: 203 0.47% 566 1.33%
4: 391 0.91% 954 2.24%
5: 513 1.20% 970 2.28%
6: 722 1.69% 1060 2.49%
7: 1177 2.75% 1136 2.66%
8: 1773 4.15% 1330 3.12%
9: 2023 4.73% 1562 3.66%
10: 2335 5.46% 1614 3.79%
11: 2682 6.27% 1861 4.37%
12: 3445 8.05% 3388 7.95%
13: 3337 7.80% 4518 10.60%
14: 3854 9.01% 1845 4.33%
15: 5329 12.46% 2853 6.69%
16: 3324 7.77% 1198 2.81%
17: 1307 3.06% 483 1.13%
18: 979 2.29% 597 1.40%
19: 1079 2.52% 643 1.51%
20: 7554 17.66% 13611 31.93%

*** Completed Phase 1 route (0:00:00.5 282.7M) ***

Total length: 2.569e+05um, number of vias: 81568
M1(H) length: 5.595e+03um, number of vias: 39631
M2(V) length: 8.589e+04um, number of vias: 31681
M3(H) length: 8.904e+04um, number of vias: 5578
M4(V) length: 3.414e+04um, number of vias: 1951
M5(H) length: 1.757e+04um, number of vias: 1279
M6(V) length: 1.917e+04um, number of vias: 426
M7(H) length: 6.145e+02um, number of vias: 385
M8(V) length: 3.170e+03um, number of vias: 258
M9(H) length: 2.047e+02um, number of vias: 211
M10(V) length: 1.096e+03um, number of vias: 168
M11(H) length: 3.887e+02um
*** Completed Phase 2 route (0:00:00.4 282.7M) ***

*** Finished all Phases (cpu=0:00:00.9 mem=282.7M) ***
Peak Memory Usage was 286.7M
*** Finished trialRoute (cpu=0:00:00.9 mem=282.7M) ***

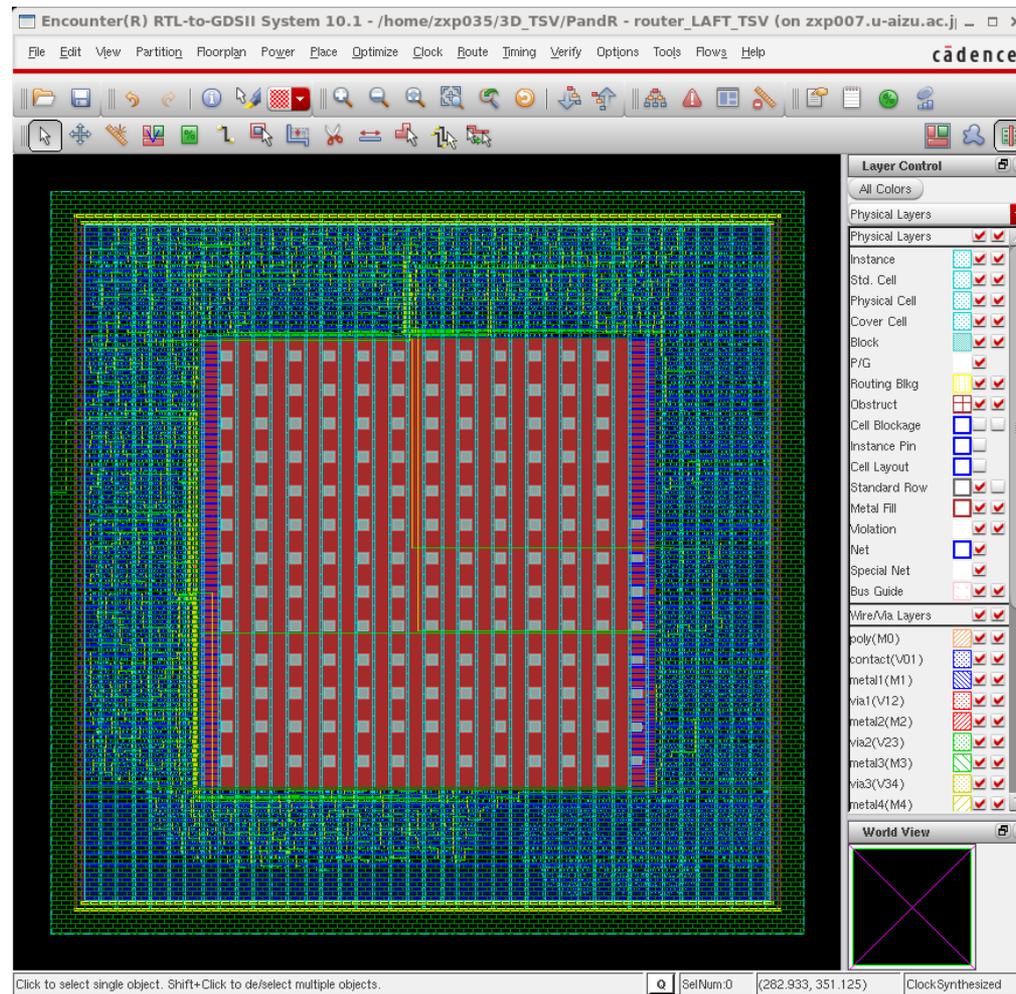
End of congRepair (cpu=0:00:05.4, real 0:00:06.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:24
***** Total real time 0:0:24
**placeDesign ... cpu = 0:0:24, real = 0:0:24, mem = 282.7M **
velocity > velocity >
```

```
#
# Step 8: Clock tree synthesis (CTS) (Clock --> Synthesize Clock Tree)
#
addCTSCellList {CLKBUF_X1 CLKBUF_X2 CLKBUF_X3}
clockDesign -genSpecOnly Clock.ctstch
clockDesign -specFile Clock.ctstch -outDir clock_report -fixedInstBeforeCTS
```

Execute the commands on the right hand in the CUI line by line to synthesize clock tree



# Step10: Clock Tree



Chip layout after synthesizing the clock tree



# Step11: Optimization

```
zxp035@zxp007:~$ cat /dev/tty
File Edit View Search Terminal Help
Max. Fall Buffer Tran. : 68.2(ps) 200(ps)
Max. Rise Sink Tran. : 101.8(ps) 200(ps)
Max. Fall Sink Tran. : 101.1(ps) 200(ps)
Min. Rise Buffer Tran. : 8.5(ps) 0(ps)
Min. Fall Buffer Tran. : 7.9(ps) 0(ps)
Min. Rise Sink Tran. : 68(ps) 0(ps)
Min. Fall Sink Tran. : 67.3(ps) 0(ps)

Clock Analysis (CPU Time 0:00:00.0)

*** None of the buffer chains at roots are modified by the fine-tune process.

#
# Mode : Setup
# Library Name : NangateOpenCellLibrary
# Operating Condition : typical
# Process : 1
# Voltage : 1.1
# Temperature : 25
#
***** Clock clk Post-CTS Timing Analysis *****
Nr. of Subtrees : 1
Nr. of Sinks : 1547
Nr. of Buffer : 47
Nr. of Level (including gates) : 3
Root Rise Input Tran : 0.1(ps)
Root Fall Input Tran : 0.1(ps)
Max trig. edge delay at sink(R): ip1/ff/fifo_reg[0][16]/CK 248.2(ps)
Min trig. edge delay at sink(R): ip6/ff/fifo_reg[3][29]/CK 228.2(ps)

Rise Phase Delay (Actual) (Required)
Fall Phase Delay : 228.2~248.2(ps) 0~10(ps)
Trig. Edge Skew : 247.7~268.1(ps) 0~10(ps)
Rise Skew : 20(ps) 20(ps)
Fall Skew : 20(ps)
Max. Rise Buffer Tran. : 20.4(ps) 200(ps)
Max. Fall Buffer Tran. : 68.8(ps) 200(ps)
Max. Rise Sink Tran. : 68.2(ps) 200(ps)
Max. Fall Sink Tran. : 101.8(ps) 200(ps)
Min. Rise Buffer Tran. : 101.1(ps) 200(ps)
Min. Fall Buffer Tran. : 8.5(ps) 0(ps)
Min. Rise Sink Tran. : 7.9(ps) 0(ps)
Min. Fall Sink Tran. : 68(ps) 0(ps)
Min. Fall Sink Tran. : 67.3(ps) 0(ps)

Generating Clock Analysis Report /outer_LAFT_TSV.ctsrpt ....
Clock Analysis (CPU Time 0:00:00.0)

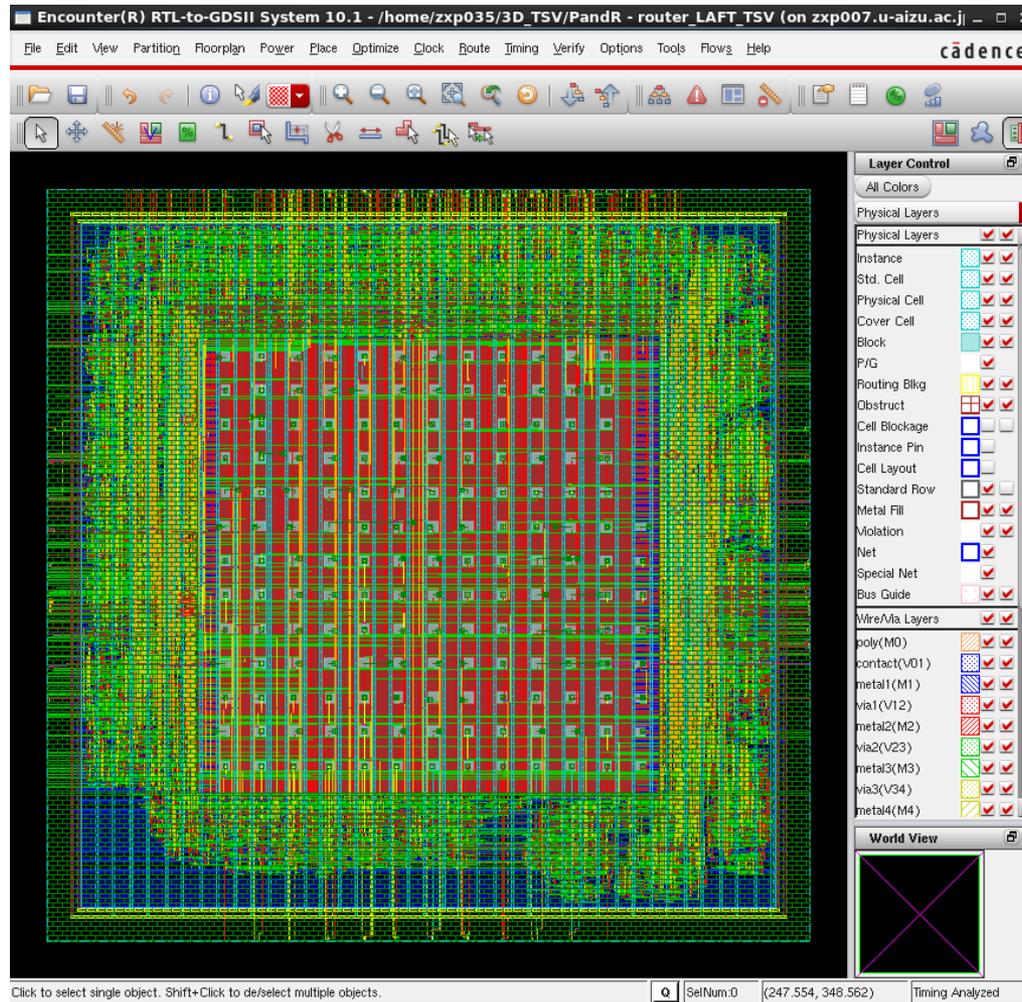
*** End ckECO (cpu=0:00:04.3, real=0:00:05.0, mem=355.0M) ***
**clockDesign ... cpu = 0:04:27, real = 0:04:27, mem = 355.0M **
velocity 11>
```

```
#
# Step 9: Optimization (postCTS) (Optimize --> Optimize Design)
#
optDesign -postCTS
optDesign -postCTS -hold
```

Execute the commands on the right hand in the CUI line by line to perform the **Post-clock synthesis optimization**



# Step11: Optimization



Chip layout after **Post-clock synthesis optimization**



# Step12: Nano Route

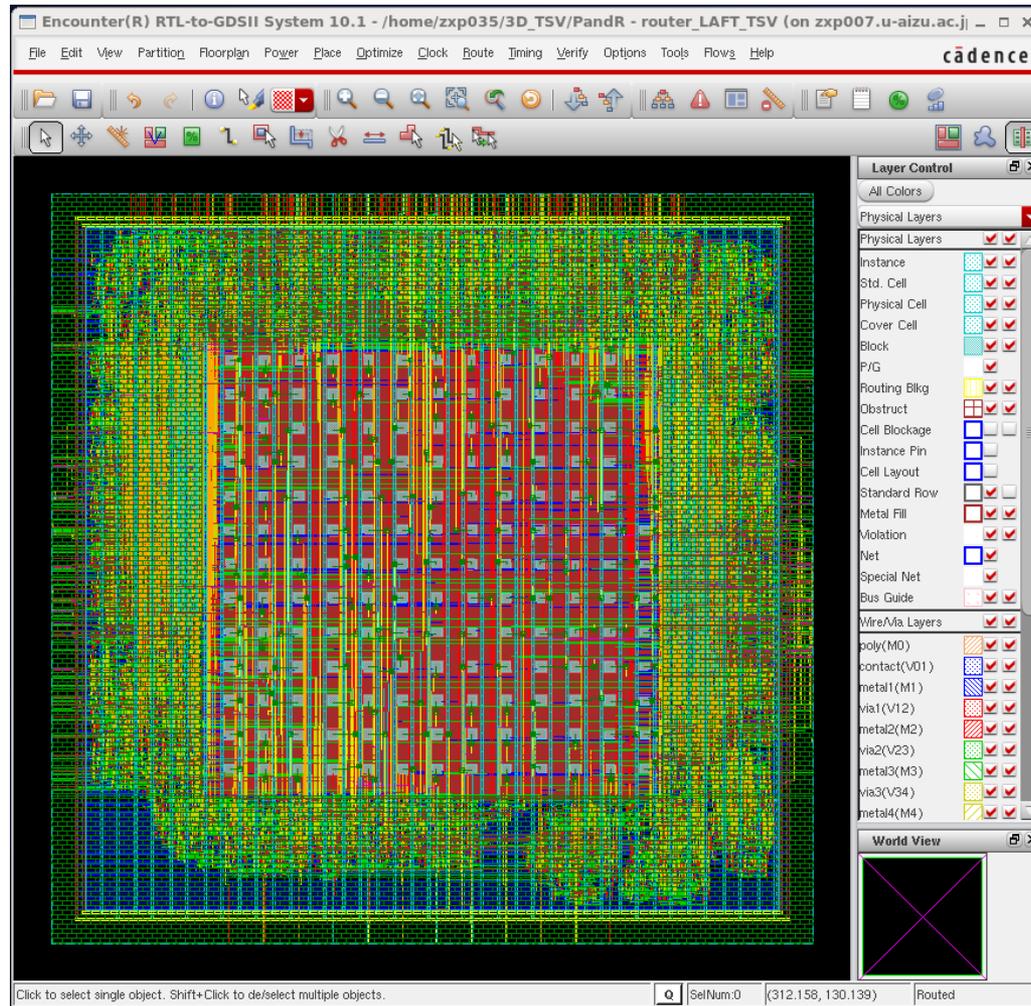
```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
#Total wire length on LAYER metal3 = 68995 um.
#Total wire length on LAYER metal4 = 40233 um.
#Total wire length on LAYER metal5 = 29043 um.
#Total wire length on LAYER metal6 = 19591 um.
#Total wire length on LAYER metal7 = 1164 um.
#Total wire length on LAYER metal8 = 4712 um.
#Total wire length on LAYER metal9 = 2420 um.
#Total wire length on LAYER metal10 = 3433 um.
#Total wire length on LAYER TM = 1101 um.
#Total number of vias = 108165
#Up-Via Summary (total 108165):
#
#-----
# Metal 1      45550
# Metal 2      40656
# Metal 3      12864
# Metal 4       5329
# Metal 5       2220
# Metal 6       561
# Metal 7       401
# Metal 8       228
# Metal 9       188
# Metal 10      168
#-----
#                    108165
#
#Total number of DRC violations = 0
#Total number of violations on LAYER metal1 = 0
#Total number of violations on LAYER metal2 = 0
#Total number of violations on LAYER metal3 = 0
#Total number of violations on LAYER metal4 = 0
#Total number of violations on LAYER metal5 = 0
#Total number of violations on LAYER metal6 = 0
#Total number of violations on LAYER metal7 = 0
#Total number of violations on LAYER metal8 = 0
#Total number of violations on LAYER metal9 = 0
#Total number of violations on LAYER metal10 = 0
#Total number of violations on LAYER TM = 0
#detailRoute Statistics:
#Cpu time = 00:00:26
#Elapsed time = 00:00:26
#Increased memory = 0.00 (Mb)
#Total memory = 363.00 (Mb)
#Peak memory = 396.00 (Mb)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:34
#Elapsed time = 00:00:34
#Increased memory = 1.00 (Mb)
#Total memory = 363.00 (Mb)
#Peak memory = 396.00 (Mb)
#Number of warnings = 10
#Total number of warnings = 78
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Wed May 27 13:30:33 2015
#
velocity 19> █
```

```
#
# Step 10: Detailed route (Route --> Nano Route --> Route)
#
setNanoRouteMode -quiet -routeWithTimingDriven true
setNanoRouteMode -quiet -routeTopRoutingLayer default
setNanoRouteMode -quiet -routeBottomRoutingLayer default
setNanoRouteMode -quiet -drouteEndIteration default
setNanoRouteMode -quiet -routeWithTimingDriven true
routeDesign -globalDetail
```

Execute the commands on the right hand in the CUI line by line to add Nano route



# Step12: Nano Route



Chip layout after **Nano-route**



# Step13: Optimization

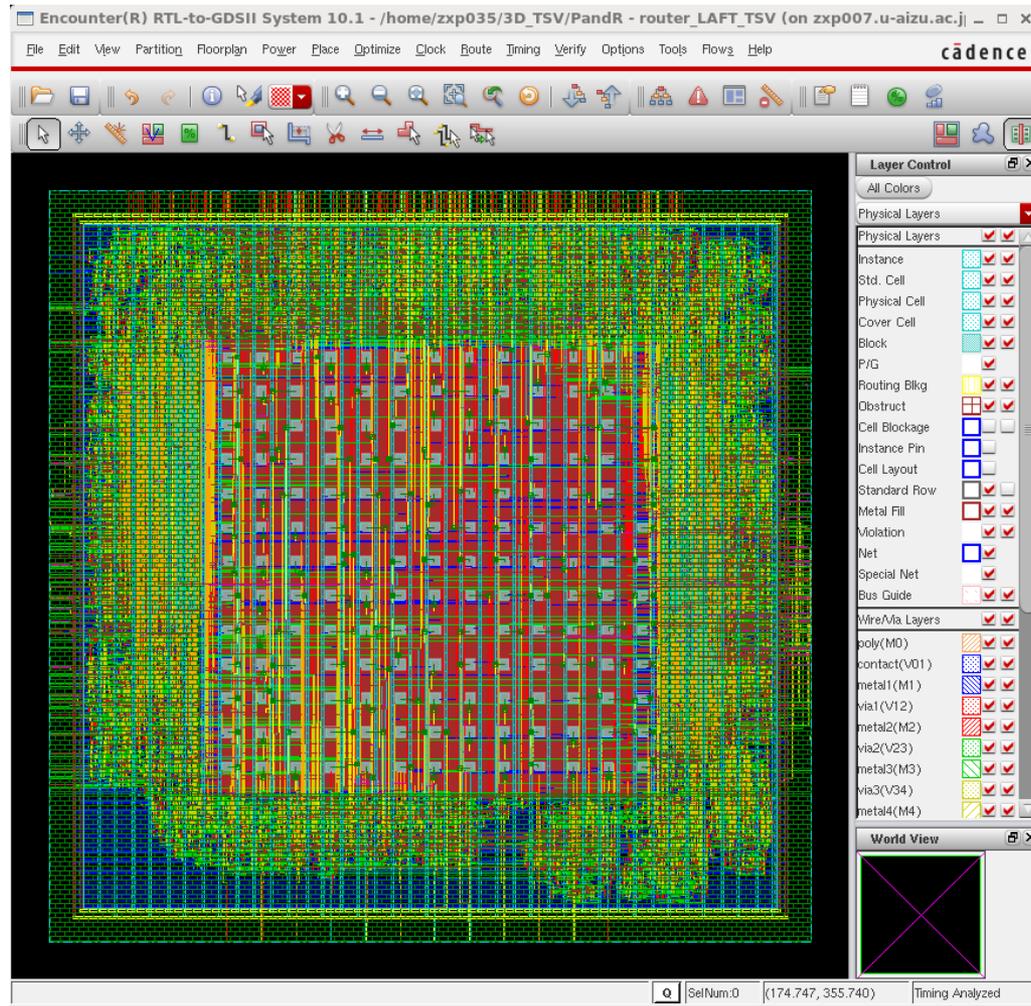
```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
#Total wire length on LAYER metal3 = 68995 um.
#Total wire length on LAYER metal4 = 40233 um.
#Total wire length on LAYER metal5 = 29043 um.
#Total wire length on LAYER metal6 = 19591 um.
#Total wire length on LAYER metal7 = 1164 um.
#Total wire length on LAYER metal8 = 4712 um.
#Total wire length on LAYER metal9 = 2420 um.
#Total wire length on LAYER metal10 = 3433 um.
#Total wire length on LAYER TM = 1101 um.
#Total number of vias = 108165
#Up-Via Summary (total 108165):
#
#-----
# Metal 1      45550
# Metal 2      40656
# Metal 3      12864
# Metal 4       5329
# Metal 5       2220
# Metal 6       561
# Metal 7       401
# Metal 8       228
# Metal 9       188
# Metal 10      168
#-----
#
#                108165
#
#Total number of DRC violations = 0
#Total number of violations on LAYER metal1 = 0
#Total number of violations on LAYER metal2 = 0
#Total number of violations on LAYER metal3 = 0
#Total number of violations on LAYER metal4 = 0
#Total number of violations on LAYER metal5 = 0
#Total number of violations on LAYER metal6 = 0
#Total number of violations on LAYER metal7 = 0
#Total number of violations on LAYER metal8 = 0
#Total number of violations on LAYER metal9 = 0
#Total number of violations on LAYER metal10 = 0
#Total number of violations on LAYER TM = 0
#detailRoute Statistics:
#Cpu time = 00:00:26
#Elapsed time = 00:00:26
#Increased memory = 0.00 (Mb)
#Total memory = 363.00 (Mb)
#Peak memory = 396.00 (Mb)
#
#globalDetailRoute statistics:
#Cpu time = 00:00:34
#Elapsed time = 00:00:34
#Increased memory = 1.00 (Mb)
#Total memory = 363.00 (Mb)
#Peak memory = 396.00 (Mb)
#Number of warnings = 10
#Total number of warnings = 70
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Wed May 27 13:30:33 2015
#
velocity 19> █
```

```
#
# Step 11: Optimization (postRoute) (Optimize --> Optimize Design)
#
optDesign -postRoute
optDesign -postRoute -hold
```

Execute the commands on the right hand in the CUI line by line to perform the **Post-route optimization**



# Step13: Optimization



Chip layout after **Post-route optimization**



# Step14: Adding Fillers

```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
# Delay Calculation Options: engine=default signOff=true SIAware=false(opt)
# Switching Delay Calculation Engine to feDC
#####
Calculate delays in Single mode...
Topological Sorting (CPU = 0:00:00.0, MEM = 430.0M, InitMEM = 430.0M)
Number of Loop : 0
Start delay calculation (mem=430.023M)...
delayCal using detail RC...
Opening parasitic data file './router_LAFT_TSV_rPEyJy_16765.rcdb.d/header.da' for reading.
RC Database In Completed (CPU Time= 0:00:00.1 MEM= 430.0M)
Delay calculation completed. (cpu=0:00:00.6 real=0:00:00.0 mem=430.035M 0)
*** CDM Built up (cpu=0:00:00.8 real=0:00:01.0 mem= 430.0M) ***
**ERROR: (ENCTS-17): Inconsistent capacitive load unit across different timing libraries, unit of lpf will be used. Use setLibraryUnit command to set consistent capacitive load unit for the design.
Reported timing to dir ./timingReports
**optDesign ... cpu = 0:00:13, real = 0:00:14, mem = 430.0M **

-----
optDesign Final Summary
-----

+-----+-----+-----+-----+-----+-----+-----+
| Setup mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+-----+-----+-----+-----+-----+-----+
| WNS (ns): | 7.827 | 7.827 | 8.797 | 8.721 | 9.531 | N/A |
| TNS (ns): | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | N/A |
| Violating Paths: | 0 | 0 | 0 | 0 | 0 | N/A |
| All Paths: | 1834 | 1547 | 1547 | 245 | 42 | N/A |
+-----+-----+-----+-----+-----+-----+-----+

+-----+-----+-----+-----+-----+-----+-----+
| Hold mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
+-----+-----+-----+-----+-----+-----+-----+
| WNS (ns): | 0.000 | 0.064 | 0.000 | 0.439 | 0.198 | N/A |
| TNS (ns): | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | N/A |
| Violating Paths: | 0 | 0 | 0 | 0 | 0 | N/A |
| All Paths: | 1834 | 1547 | 1547 | 245 | 42 | N/A |
+-----+-----+-----+-----+-----+-----+-----+

+-----+-----+-----+-----+-----+-----+-----+
| DRVs | | Real | | Total |
| | | Nr nets(terms) | | Worst Vio | | Nr nets(terms) |
+-----+-----+-----+-----+-----+-----+-----+
| max_cap | | 0 (0) | | 0.000 | | 0 (0) |
| max_tran | | 0 (0) | | 0.000 | | 0 (0) |
| max_fanout | | 0 (0) | | 0 | | 0 (0) |
+-----+-----+-----+-----+-----+-----+-----+

Density: 37.754%

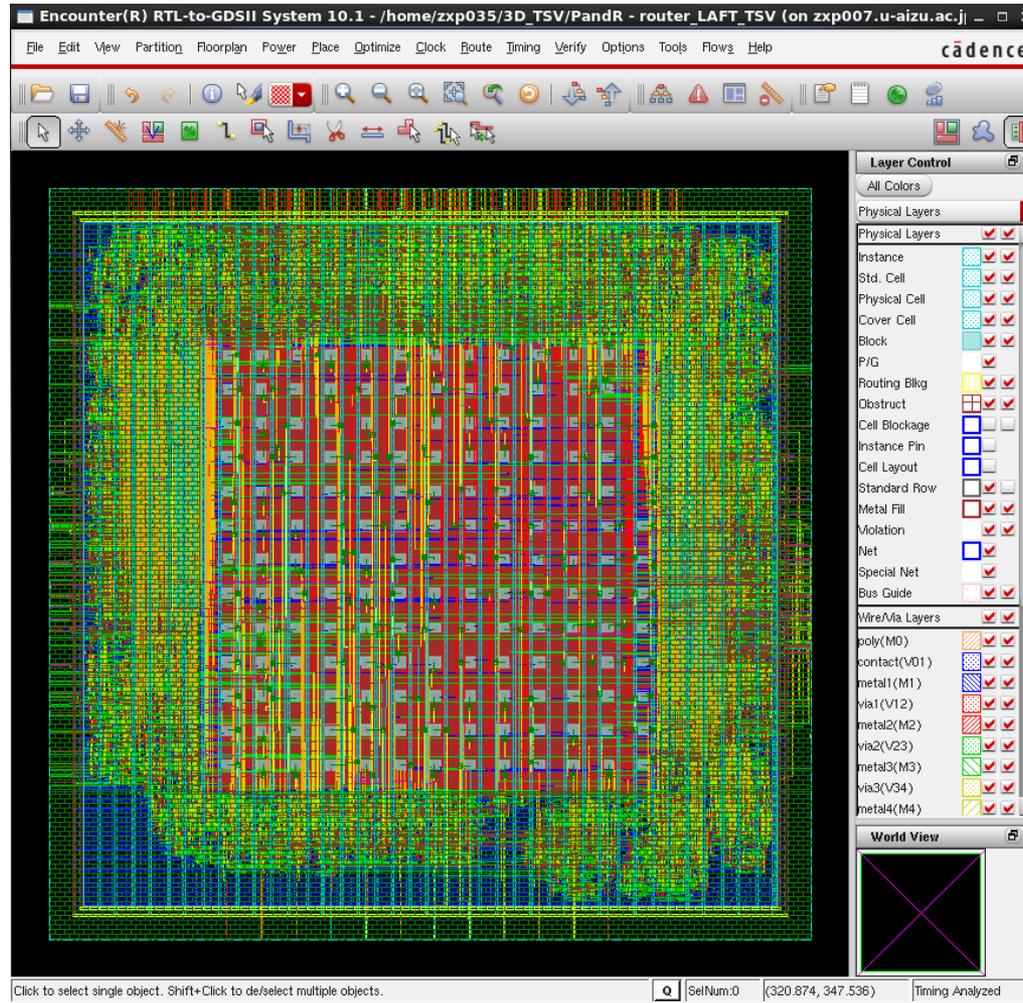
*** Final Summary (holdfix) CPU=0:00:01.7, REAL=0:00:02.0, TOTCPU=0:00:12.8, TOTREAL=0:00:14.0, MEM=426.3M
**optDesign ... cpu = 0:00:14, real = 0:00:16, mem = 426.3M **
*** Finished optDesign ***
velocity 26> █
```

```
#
# Step 12: Add fillers (Place --> Physical Cells --> Add Filler)
#
addFiller -prefix FILLER -cell FILLCELL_X1 FILLCELL_X2 FILLCELL_X4 \
FILLCELL_X8 FILLCELL_X16 FILLCELL_X32
```

Execute the commands on the right hand in the CUI line by line to add fillers



# Step14: Adding Fillers



Chip layout after adding fillers



# Step15: Layout Vs. Schematic(LVS)

```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
-----
WNS (ns):| 7.827 | 7.827 | 8.797 | 8.721 | 9.531 | N/A |
TNS (ns):| 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | N/A |
Violating Paths:| 0 | 0 | 0 | 0 | 0 | N/A |
All Paths:| 1834 | 1547 | 1547 | 245 | 42 | N/A |
-----
Hold mode | all | reg2reg | in2reg | reg2out | in2out | clkgate |
-----
WNS (ns):| 0.000 | 0.064 | 0.000 | 0.439 | 0.198 | N/A |
TNS (ns):| 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | N/A |
Violating Paths:| 0 | 0 | 0 | 0 | 0 | N/A |
All Paths:| 1834 | 1547 | 1547 | 245 | 42 | N/A |
-----
DRVs | Real | Total |
-----
Nr nets(terms) | Worst Vio | Nr nets(terms) |
-----
max_cap | 0 (0) | 0.000 | 0 (0) |
max_tran | 0 (0) | 0.000 | 0 (0) |
max_fanout | 0 (0) | 0 | 0 (0) |
-----
Density: 37.754%
*** Final Summary (holdfix) CPU=0:00:01.7, REAL=0:00:02.0, TOTCPU=0:00:12.8, TOTREAL=0:00:14.0, MEM=426.3M
**optDesign ... cpu = 0:00:14, real = 0:00:16, mem = 426.3M **
*** Finished optDesign ***
velocity 26> velocity 26> addFiller -prefix FILLER -cell FILLCELL_X1 FILLCELL_X2 FILLCELL_X4 \
+ FILLCELL_X8 FILLCELL_X16 FILLCELL_X32
*INFO: Adding fillers to top-module.
*INFO: Added 951 filler insts (cell FILLCELL_X32 / prefix FILLER).
*INFO: Added 1357 filler insts (cell FILLCELL_X16 / prefix FILLER).
*INFO: Added 3389 filler insts (cell FILLCELL_X8 / prefix FILLER).
*INFO: Added 5259 filler insts (cell FILLCELL_X4 / prefix FILLER).
*INFO: Added 15523 filler insts (cell FILLCELL_X1 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILLCELL_X2 / prefix FILLER).
*INFO: Total 26479 filler insts added - prefix FILLER (CPU: 0:00:00.1).
*** Applied 0 GNC rules (cpu = 0:00:00.0)
*INFO: Checking for DRC violations on added fillers.
**WARN: (ENCVFG-12): SPACING SAMENET value 800 has been defined on M7 layer, value 800 will be ignored.
**WARN: (ENCVFG-12): SPACING SAMENET value 800 has been defined on M8 layer, value 800 will be ignored.
**WARN: (ENCVFG-47): Pin of Cell FILLER_290 at (15.010, 20.525), (21.090, 20.695) on Layer metal1 is not connected to any net. Use globalNetConnect or GUI FloorPlan->Connect Global Nets to specify global net connection rules properly.
*INFO: Iteration 0-#1, Found 0 DRC violation (real: 0:00:01.0).
*INFO: Adding fillers to top-module.
*INFO: Added 0 filler inst of any cell-type.
*** Applied 0 GNC rules (cpu = 0:00:00.0)
*INFO: End DRC Checks. (real: 0:00:01.0)
velocity 27>
```

```
#
# Step 13: Verification (LVS) (Verify --> Verify Connectivity)
#
verifyConnectivity -type all -error 1000 -warning 50
```

Execute the commands on the right hand in the CUI line by line to perform the **LVS check**



# Step15: Layout Vs. Schematic(LVS)

```
***** Start: VERIFY CONNECTIVITY *****
Start Time: Wed May 27 13:34:30 2015

Design Name: router_LAFT_TSV
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (330.0100, 330.0100)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 13:34:30 **** Processed 5000 nets (Total 13442)
**** 13:34:30 **** Processed 10000 nets (Total 13442)
Time Elapsed: 0:00:00.0

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Wed May 27 13:34:30 2015
***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.5 MEM: 0.004M)
```

LVS check report on the CUI  
Successful check (No errors and no warning)





# Step16: Design Rule Check(DRC)

```
VERIFY GEOMETRY ..... Cells           : 0 Viols.
VERIFY GEOMETRY ..... SameNet          : 0 Viols.
VERIFY GEOMETRY ..... Wiring           : 0 Viols.
VERIFY GEOMETRY ..... Antenna           : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 2 of 4
VERIFY GEOMETRY ..... Cells           : 0 Viols.
VERIFY GEOMETRY ..... SameNet          : 0 Viols.
VERIFY GEOMETRY ..... Wiring           : 0 Viols.
VERIFY GEOMETRY ..... Antenna           : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 2 complete 0 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 3 of 4
VERIFY GEOMETRY ..... Cells           : 0 Viols.
VERIFY GEOMETRY ..... SameNet          : 0 Viols.
VERIFY GEOMETRY ..... Wiring           : 0 Viols.
VERIFY GEOMETRY ..... Antenna           : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 3 complete 0 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 4 of 4
VERIFY GEOMETRY ..... Cells           : 0 Viols.
VERIFY GEOMETRY ..... SameNet          : 0 Viols.
VERIFY GEOMETRY ..... Wiring           : 0 Viols.
VERIFY GEOMETRY ..... Antenna           : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 4 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 2.00
Begin Summary ...
Cells           : 0
SameNet         : 0
Wiring          : 0
Antenna         : 0
Short           : 0
Overlap         : 0
End Summary
Verification Complete : 0 Viols. 0 Wrngs.
```

DRC check report on the CUI  
Successful check (No violations and no warning)



# Step17: Output files

```
zxp035@zxp007:PandR
File Edit View Search Terminal Help
(CPU Time: 0:00:00.5 MEM: 0.004M)

velocity 28> verifyGeometry
*** Starting Verify Geometry (MEM: 476.7) ***

VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
**WARN: (ENCVFG-12): SPACING SAMENET value 880 has been defined on M7 layer, value
800 will be ignored.
**WARN: (ENCVFG-12): SPACING SAMENET value 880 has been defined on M8 layer, value
800 will be ignored.
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
..... bin size: 2080
VERIFY GEOMETRY ..... SubArea : 1 of 4
**WARN: (ENCVFG-47): Pin of Cell FILLER_292 at (28.010, 20.525), (29.010, 20.695)
on Layer metal1 is not connected to any net. Use globalNetConnect or GUI FloorPlan->C
onnect Global Nets to specify global net connection rules properly.

VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 2 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 2 complete 0 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 3 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 3 complete 0 Viols. 0 Wrngs.
VERIFY GEOMETRY ..... SubArea : 4 of 4
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 4 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 2.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:02.3 MEM: 45.8M)

velocity 29> []
```

```
#
# Step 15: Data out (Timing --> Extract RC, Timing --> Write SDF,
# File --> Save --> Netlist)
saveNetlist output_files/router_LAFT_macroTSV_final.vnet
isExtractRCModeSignoff
rcOut -spef output_files/router_LAFT_macroTSV.spef
delayCal -sdf output_files/router_LAFT_macroTSV.sdf -idealclock
saveDesign router_LAFT_macroTSV_final.enc
```

Execute the commands on the right hand in the CUI line by line to generate the **output files** and **finish P&R**



# PandR.tcl script (1/5)

```
#  
# Step 1: Setup (File --> Import Design)  
#  
setUIVar rda_Input ui_netlist vnet/router_LAFT_TSV.vnet  
setUIVar rda_Input ui_timingcon_file ../Syn/output_files/router_LAFT_TSV.sdc  
setUIVar rda_Input ui_topcell router_LAFT_TSV  
setUIVar rda_Input ui_leffile {macro/TSV.lef /home/zxp035/lib/NangateOpenCellLibrary.lef}  
setUIVar rda_Input ui_timelib {/home/zxp035/lib/typical.lib macro/TSV.lib}  
  
setUIVar rda_Input ui_pwrnet VDD  
setUIVar rda_Input ui_gndnet VSS  
setUIVar rda_Input ui_cts_cell_list {CLKBUF_X1 CLKBUF_X2 CLKBUF_X3}  
commitConfig  
win  
  
floorPlan -s 300 300 15 15 15 15  
#set halo#  
addHaloToBlock 0.5 0.5 0.5 0.5 -allBlock  
  
createRouteBlk -box 0 0 380 65 -layer 11  
createRouteBlk -box 0 65 65 265 -layer 11  
createRouteBlk -box 265 65 380 265 -layer 11  
createRouteBlk -box 0 265 380 380 -layer 11  
  
#place macro  
placeInstance tsv_input_up0 75 75 R0  
placeInstance tsv_input_up1 75 90 R0  
placeInstance tsv_input_up2 75 105 R0  
placeInstance tsv_input_up3 75 120 R0  
placeInstance tsv_input_up4 75 135 R0  
placeInstance tsv_input_up5 75 150 R0  
placeInstance tsv_input_up6 75 165 R0  
placeInstance tsv_input_up7 75 180 R0  
placeInstance tsv_input_up8 75 195 R0  
placeInstance tsv_input_up9 75 210 R0  
placeInstance tsv_input_up10 75 225 R0  
placeInstance tsv_input_up11 75 240 R0  
placeInstance tsv_input_up12 75 255 R0
```



# *PandR.tcl* script (2/5)

```
placeInstance tsv_faulty_output_up0 225 255 R0
placeInstance tsv_faulty_output_down0 240 75 R0
placeInstance tsv_faulty_input_up1 240 90 R0
placeInstance tsv_faulty_input_down1 240 105 R0
placeInstance tsv_faulty_output_up1 240 120 R0
placeInstance tsv_faulty_output_down1 240 135 R0
placeInstance tsv_faulty_input_up2 240 150 R0
placeInstance tsv_faulty_input_down2 240 165 R0
placeInstance tsv_faulty_output_up2 240 180 R0
placeInstance tsv_faulty_output_down2 240 195 R0
placeInstance tsv_faulty_input_up3 240 210 R0
placeInstance tsv_faulty_input_down3 240 225 R0
placeInstance tsv_faulty_output_up3 240 240 R0
placeInstance tsv_faulty_output_down3 240 255 R0

placeInstance tsv_faulty_input_up4 255 75 R0
placeInstance tsv_faulty_input_down4 255 90 R0
placeInstance tsv_faulty_output_up4 255 105 R0
placeInstance tsv_faulty_output_down4 255 120 R0
placeInstance tsv_faulty_input_up5 255 135 R0
placeInstance tsv_faulty_input_down5 255 150 R0
placeInstance tsv_faulty_output_up5 255 165 R0
placeInstance tsv_faulty_output_down5 255 180 R0

createObstruct 65 65 265 265

# Place your hard-macro manually

#saveDesign floor.enc

#
# Step 3: Power ring (Power --> Power Planning --> Add Ring)
#
createPGPin VDD -net VDD
createPGPin VSS -net VSS
```



# PandR.tcl script (3/5)

```
addRing -nets {VSS VDD} -type core_rings \  
-spacing_top 2 -spacing_bottom 2 -spacing_right 2 -spacing_left 2 \  
-width_top 1 -width_bottom 1 -width_right 1 -width_left 1 \  
-around_core -jog_distance 0.095 -threshold 0.095 \  
-layer_top metal10 -layer_bottom metal10 -layer_right metal9 \  
-layer_left metal9 \  
-stacked_via_top_layer metal10 -stacked_via_bottom_layer metal1  
  
#  
# Step 4: Power stripe (Power --> Power Planning --> Add Stripe)  
#  
addStripe -nets {VSS VDD} -layer metal8 -width 1 -spacing 6 \  
-block_ring_top_layer_limit metal9 -block_ring_bottom_layer_limit metal7 \  
-padcore_ring_top_layer_limit metal9 -padcore_ring_bottom_layer_limit metal7 \  
-stacked_via_top_layer metal10 -stacked_via_bottom_layer metal1 \  
-set_to_set_distance 15 -xleft_offset 6 -merge_stripes_value 0.095 \  
-max_same_layer_jog_length 1.6  
  
#  
# Step 5: Power route (Route --> Special Router)  
#  
sroute -nets {VSS VDD} -layerChangeRange {1 10} \  
-connect { blockPin padPin padRing corePin floatingStripe } \  
-blockPinTarget { nearestRingStripe nearestTarget } \  
-padPinPortConnect { allPort oneGeom } \  
-checkAlignedSecondaryPin 1 -blockPin useLef -allowJogging 1 \  
-crossoverViaBottomLayer 1 -allowLayerChange 1 -targetViaTopLayer 10 \  
-crossoverViaTopLayer 10 -targetViaBottomLayer 1  
  
#  
# Step 6: Placement (Place --> Standard Cell)  
#  
placeDesign -prePlaceOpt  
  
#  
# Step 7: Optimization (preCTS) (Optimize --> Optimize Design)  
#  
optDesign -preCTS
```



# *PandR.tcl* script (4/5)

---

```
#
# Step 8: Clock tree synthesis (CTS) (Clock --> Synthesize Clock Tree)
#
addCTSCellList {CLKBUF_X1 CLKBUF_X2 CLKBUF_X3}
clockDesign -genSpecOnly Clock.ctstch
clockDesign -specFile Clock.ctstch -outDir clock_report -fixedInstBeforeCTS

#
# Step 9: Optimization (postCTS) (Optimize --> Optimize Design)
#
optDesign -postCTS
optDesign -postCTS -hold

#
# Step 10: Detailed route (Route --> Nano Route --> Route)
#
setNanoRouteMode -quiet -routeWithTimingDriven true
setNanoRouteMode -quiet -routeTopRoutingLayer default
setNanoRouteMode -quiet -routeBottomRoutingLayer default
setNanoRouteMode -quiet -drouteEndIteration default
setNanoRouteMode -quiet -routeWithTimingDriven true
routeDesign -globalDetail

#
# Step 11: Optimization (postRoute) (Optimize --> Optimize Design)
#
optDesign -postRoute
optDesign -postRoute -hold
```



# *PandR.tcl* script (5/5)

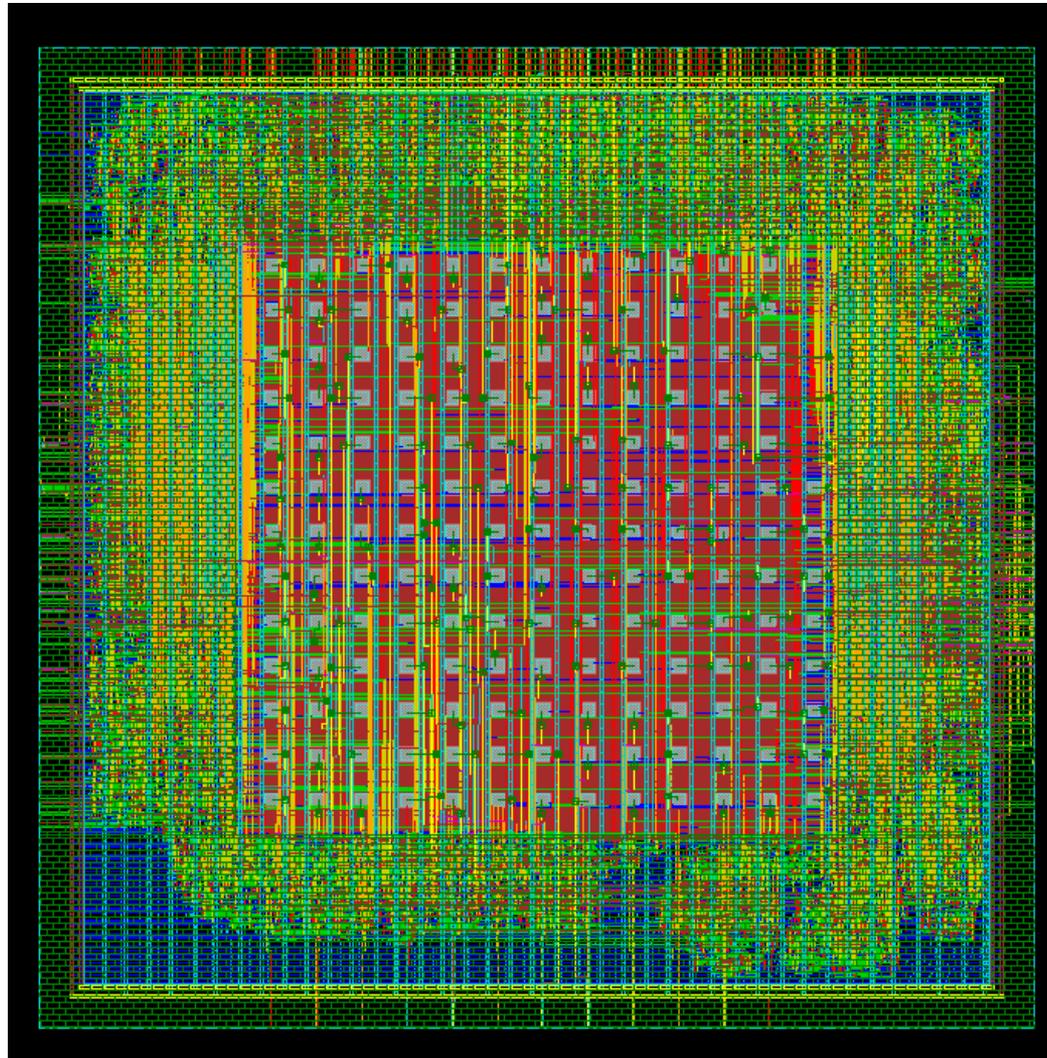
---

```
#
# Step 12: Add fillers (Place --> Physical Cells --> Add Filler)
#
addFiller -prefix FILLER -cell FILLCELL_X1 FILLCELL_X2 FILLCELL_X4 \
  FILLCELL_X8 FILLCELL_X16 FILLCELL_X32
#
# Step 13: Verification (LVS) (Verify --> Verify Connectivity)
#
verifyConnectivity -type all -error 1000 -warning 50
#
# Step 14: Verification (DRC) (Verify --> Verify Geometry)
#
verifyGeometry
#
# Step 15: Data out (Timing --> Extract RC, Timing --> Write SDF,
#               File --> Save --> Netlist)
saveNetlist output_files/router_LAFT_macroTSV_final.vnet
isExtractRCModeSignoff
rcOut -spef output_files/router_LAFT_macroTSV.spef
delayCal -sdf output_files/router_LAFT_macroTSV.sdf -idealclock

saveDesign router_LAFT_macroTSV_final.enc
```



# Final chip layout





# References

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- [Ref.1] A. Ben Ahmed, A. Ben Abdallah, [OASIS 3D-Router Hardware Physical Design](#), Technical Report, Adaptive Systems Laboratory, Division of Computer Engineering, School of Computer Science and Engineering, University of Aizu, July 8, 2014.
- [Ref.2] A. Ben Ahmed, A. Ben Abdallah, [Graceful Deadlock-Free Fault-Tolerant Routing Algorithm for 3D Network-on-Chip Architectures](#), Journal of Parallel and Distributed Computing 74/4 (2014), pp. 2229-2240.
- [Ref.3] <http://www.eda.ncsu.edu/wiki/FreePDK3D45:Manual>



# Acknowledgement

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